

AM64x/AM243x GENERAL PURPOSE EVM BOARD
PROC101C

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REV	C
VER	1.1



REVISION HISTORY

VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
0.1	11th MARCH 2022	Drafted from "PROC101B_SCH" document.	Mistral Design Team	AJIT MB	AJIT MB
0.2	11th MARCH 2022	Removed Voltage Monitor circuit & added RC Delay Circuit for power down sequence requirement Fixed Power down sequence issue seen on AM243x REV B	Mistral Design Team	AJIT MB	AJIT MB
0.3	11th MARCH 2022	Updated schematics to support PG2 Silicon	Mistral Design Team	AJIT MB	AJIT MB
1.0	30th MARCH 2022	Baselined and Released	Mistral Design Team	AJIT MB	AJIT MB
1.1	16th AUG 2022	Symbol Updated to Match Datasheet Pin Names	Mistral Design Team	AJIT MB	AJIT MB

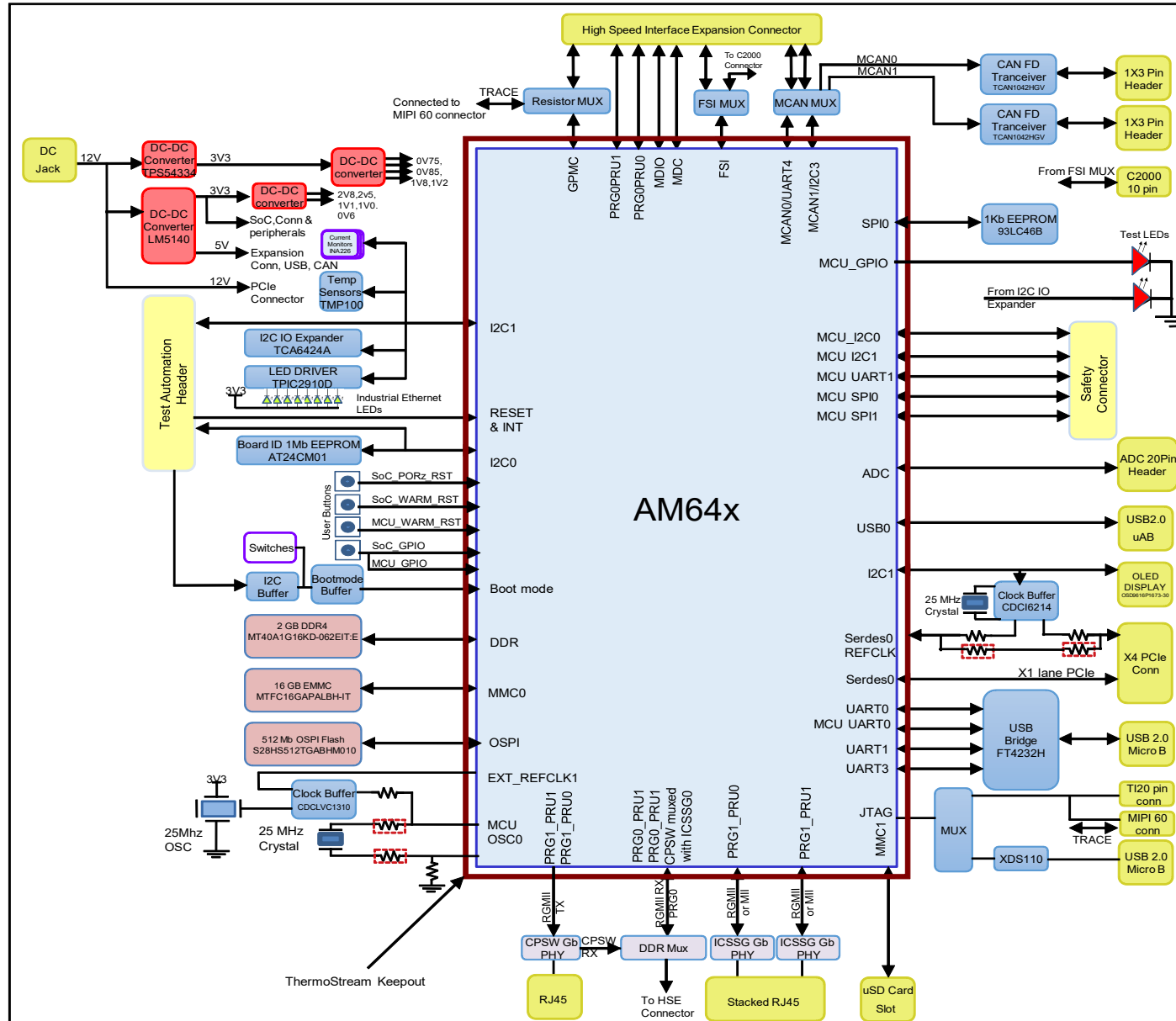
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Title REVISION HISTORY

Size	Variant Name = PROC101C(002) TMD5243GPEVM	Rev
C		E2
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BLOCK DIAGRAM_AM64x_EVM



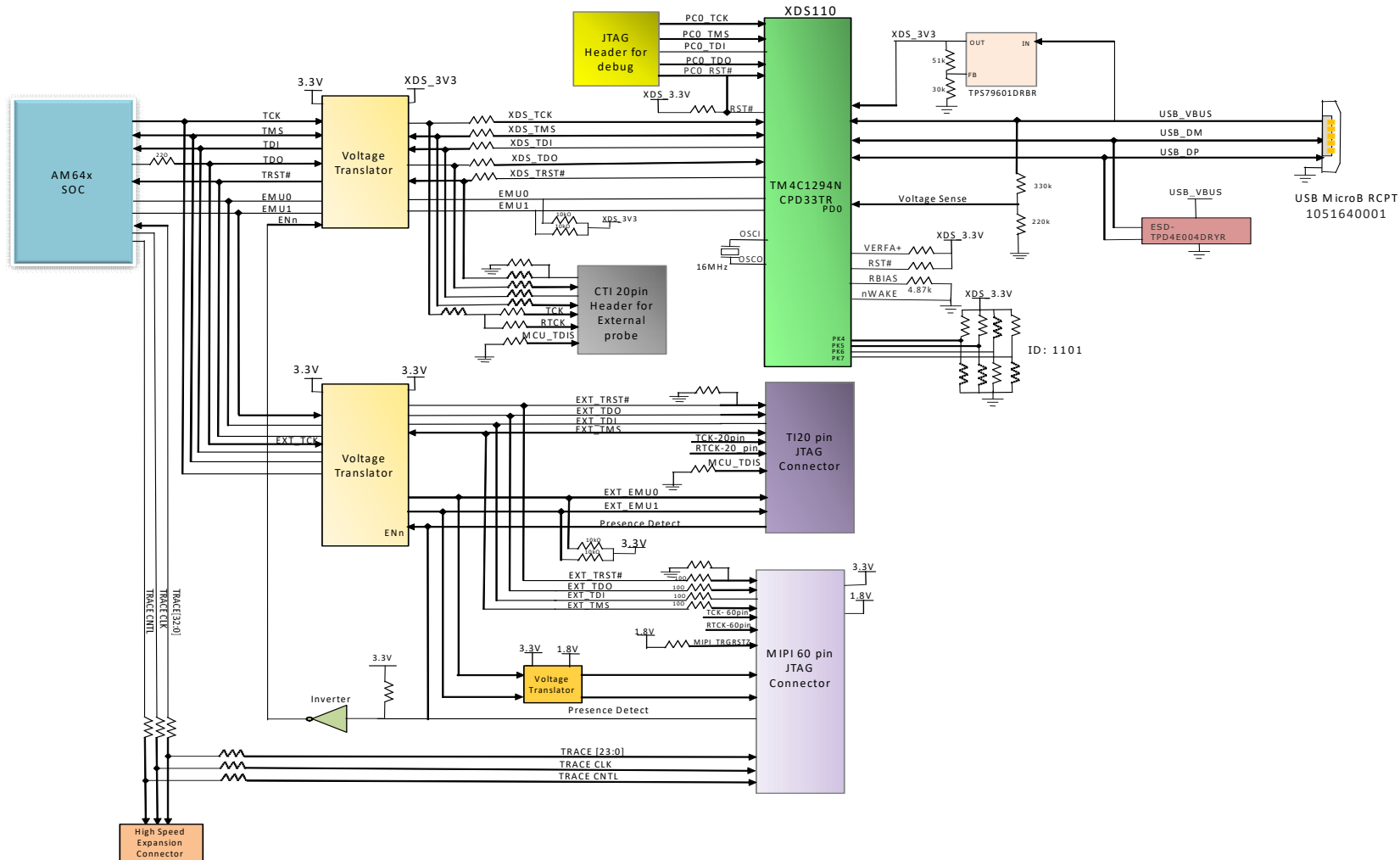
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Title	BLOCK DIAGRAM_CP BOARD
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Size	Variant Name = PROC101C(002) TMD5243GPEVM	Rev
C		E2
Date: Monday, August 22, 2022	Sheet 3 of 40	

BLOCK DIAGRAM_XDS110



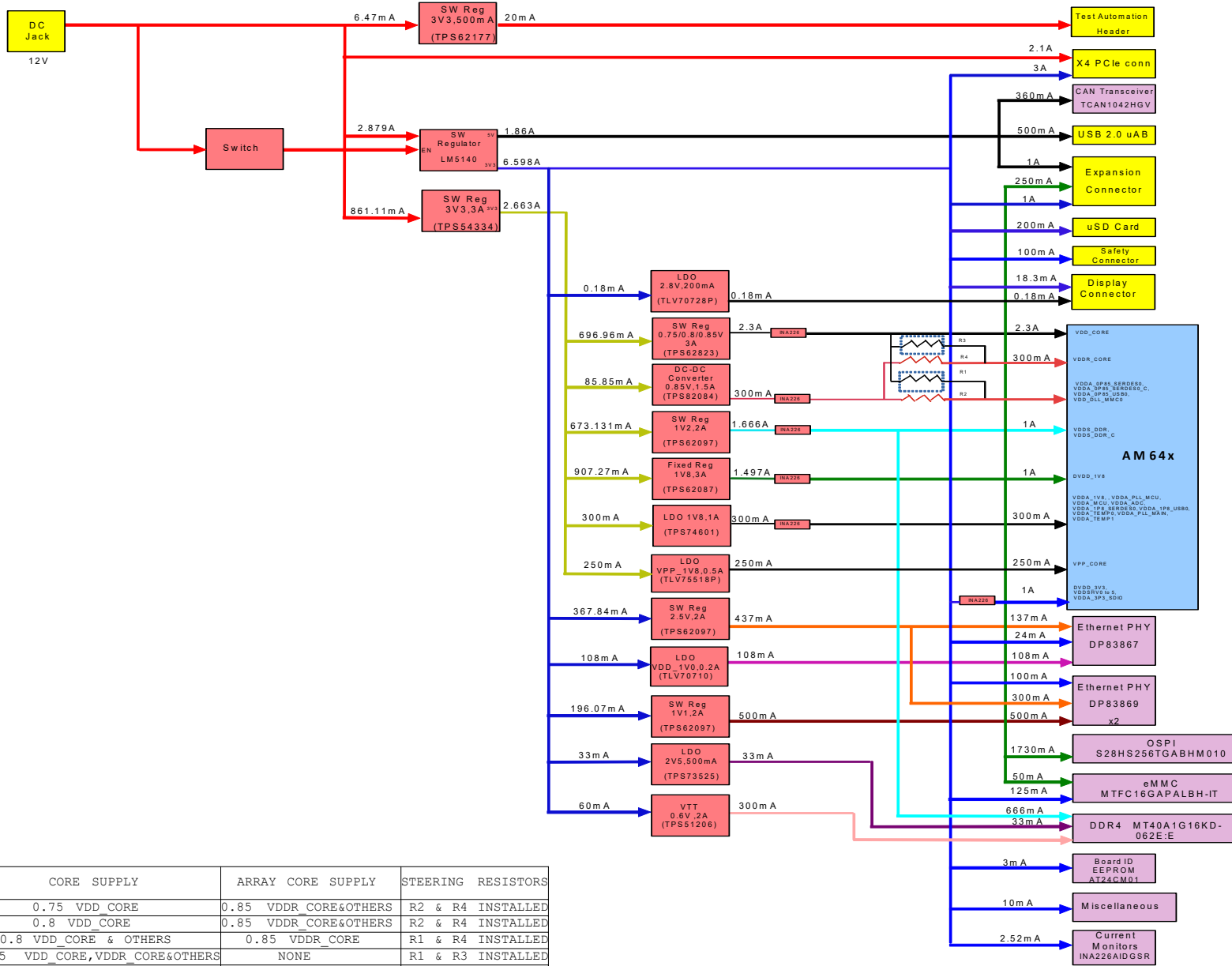
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Title BLOCK DIAGRAM_XDS110

Size	Variant Name = PROC101C(002) TMD5243GPEVM	Rev
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POWER FLOW DIAGRAM



CORE SUPPLY	ARRAY CORE SUPPLY	STEERING RESISTORS
0.75 VDD_CORE	0.85 VDDR_CORE&OTHERS	R2 & R4 INSTALLED
0.8 VDD_CORE	0.85 VDDR_CORE&OTHERS	R2 & R4 INSTALLED
0.8 VDD_CORE & OTHERS	0.85 VDDR_CORE	R1 & R4 INSTALLED
0.85 VDD_CORE, VDDR_CORE&OTHERS	NONE	R1 & R3 INSTALLED

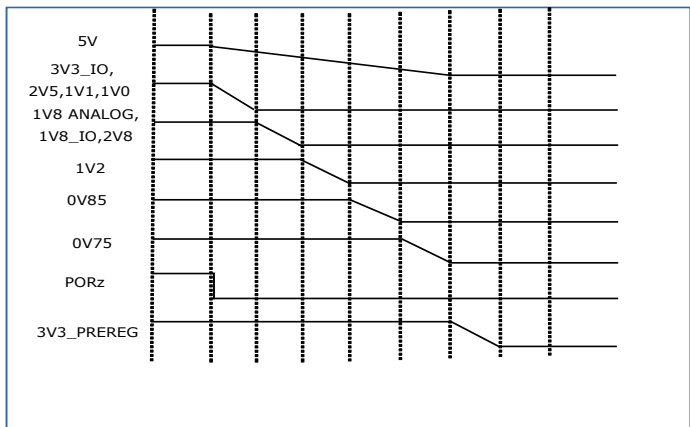
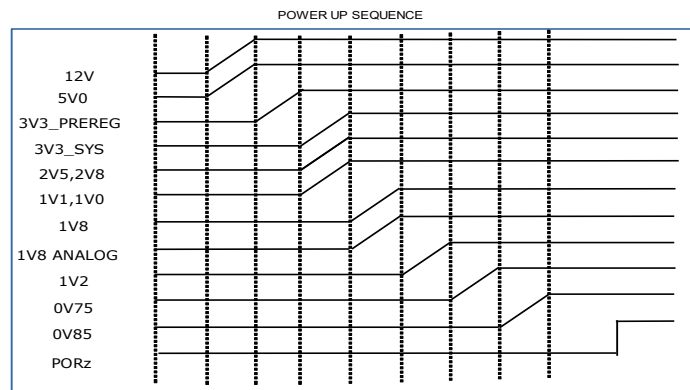
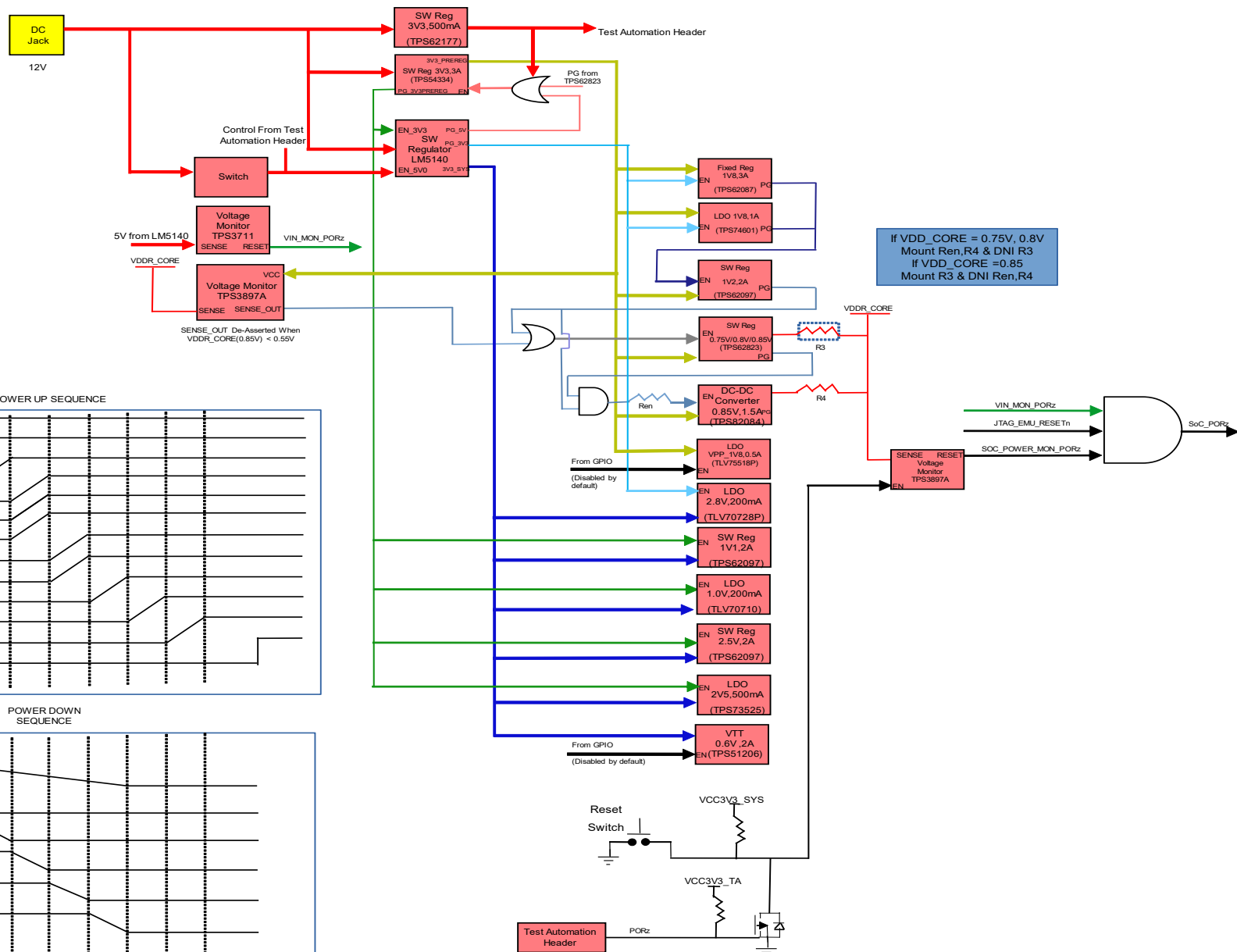
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Title POWER FLOW DIAGRAM

Size	Variant Name = PROC101C(002) TMD5243GPEVM	Rev
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POWER SEQUENCE



GPIO MAPPING TABLE

S.NO	GPIO DESCRIPTION	GPIO NETNAME	REQUIRED ON	FUNCTIONALITY	GPIO USED	SoC Muxed Signal Name	DIRECTION WITH RESPECT TO CONTROL	DEFAULT STATE	ACTIVE STATE
1	EMMC RESET Control GPIO	GPIO_eMMC_RSTn	GP EVM	Reset	IO EXPANDER- P00		OUTPUT	HIGH	LOW
2	OSPI RESET Control GPIO	GPIO_OSPI_RSTn	GP EVM	Reset	GPIO013	OSPI0_CS2	OUTPUT	HIGH	LOW
3	CPSW RGMII1 RESET Control GPIO	GPIO_CPSW1_RST	GP EVM	Reset	IO EXPANDER- P02		OUTPUT	HIGH	LOW
4	PRG1 RGMII1 Ethernet PHY RESET Control GPIO	GPIO_RGMII1_RST	GP EVM	Reset	IO EXPANDER- P03		OUTPUT	HIGH	LOW
5	PRG1 RGMII2 Ethernet PHY RESET Control GPIO	GPIO_RGMII2_RST	GP EVM	Reset	IO EXPANDER- P04		OUTPUT	HIGH	LOW
6	PRG1 RGMII1 Ethernet PHY Link Detection GPIO	PRG1_ETH1_LED_LINK	GP EVM	Link Detection	PRG1_PRU0_GPO8		INPUT	LOW	HIGH
7	PRG1 RGMII2 Ethernet PHY Link Detection GPIO	PRG1_ETH2_LED_LINK	GP EVM	Link Detection	PRG1_PRU1_GPO8		INPUT	LOW	HIGH
8	CPSW Ethernet PHY Interrupt	CPSW_RGMII_INTn	GP EVM	Interrupt	Connected to PRG1_RGMII_INT via OE res		INPUT	HIGH	LOW
9	PRG1 Ethernet PHY 1Interrupt	PRG1_RGMII_INT	GP EVM	Interrupt	GPIO1_70	EXTINTn	INPUT	HIGH	LOW
10	PRG1 Ethernet PHY 2Interrupt			Interrupt			INPUT	HIGH	LOW
11	PCIe RESET Control GPIO	GPIO_PCl_e_RST_OUT	GP EVM	Reset	IO EXPANDER- P05		OUTPUT	LOW	HIGH
12	SD card load switch enable control	MMC1_SD_EN	GP EVM	Load SW Enable	IO EXPANDER- P06		OUTPUT	HIGH	LOW
13	One GPIO is required to control the Mux select between HSE and FSI Connector	FSI_FET_SEL	GP EVM	Mux Selection	IO EXPANDER- P07		OUTPUT	PREFERABLE	PREFERABLE
14	One GPIO is required to enable Standby mode in CAN transceiver	MCAN0_STB_3V3	GP EVM	Standby mode selection	IO EXPANDER- P10		OUTPUT	LOW	HIGH
15	One GPIO is required to enable Standby mode in CAN transceiver	MCAN1_STB_3V3	GP EVM	Standby mode selection	IO EXPANDER- P11		OUTPUT	LOW	HIGH
16	One GPIO is required to control the Mux select between HSE and Ethernet PHY	CPSW_FET_SEL	GP EVM	Mux Selection	IO EXPANDER- P12		OUTPUT	PREFERABLE	PREFERABLE
17	MDC/MDIO FET Switch Select for Mux	PRG1_RGMII2_FET_SEL	GP EVM	Mux Selection	IO EXPANDER- P14		OUTPUT	PREFERABLE	PREFERABLE
18	VTT 0.6V regulator Enable	VTT_EN	GP EVM	VTT 0.6V regulator Enable	GPIO0_12	OSPI0_CSn1	OUTPUT	LOW	HIGH
19	TEST GPIO1 from Test Automation Connector/ GPIO for GP board push button	TEST GPIO1/GPIO1_43	GP EVM	GPIO for communications with AM64x	GPIO1_43	SPI0_CS1	INPUT	HIGH	LOW
20	TEST GPIO2 from Test Automation Connector	TEST GPIO2	GP EVM	GPIO for communications with AM64x	IO EXPANDER- P15		INPUT	HIGH	LOW
21	OLED Display RESET GPIO	GPIO_OLED_RESEtN	GP EVM	Reset	IO EXPANDER- P16		OUTPUT	LOW	HIGH
22	IO Expander Interrupt	IO_EXP_INTn	GP EVM	Interrupt	GPIO1_78	MMC1_SDWP	INPUT	HIGH	LOW
23	VPP 1.8V regulator Enable	VPP_LDO_EN	GP EVM	VPP 01.8V regulator Enable	IO EXPANDER- P17		OUTPUT	LOW	HIGH
24	One GPIO is required to control the Mux select between HSE and CAN Interface	CAN_MUX_SEL	GP EVM	Mux Selection	IO EXPANDER- P01		OUTPUT	LOW	HIGH
25	User LED	TEST_LED1	GP EVM	Test	IO EXPANDER- P20		OUTPUT	LOW	HIGH
26	User LED	TEST_LED2	GP EVM	Test	MCU_SPI1_CS0	MCU_GPIO0_5	OUTPUT	LOW	HIGH
27	One GPIO to enable the PCIe Clock generator outputs	CDC_OE1/E4	GP EVM	Clock output enable	IO EXPANDER- P21		OUTPUT	HIGH	HIGH

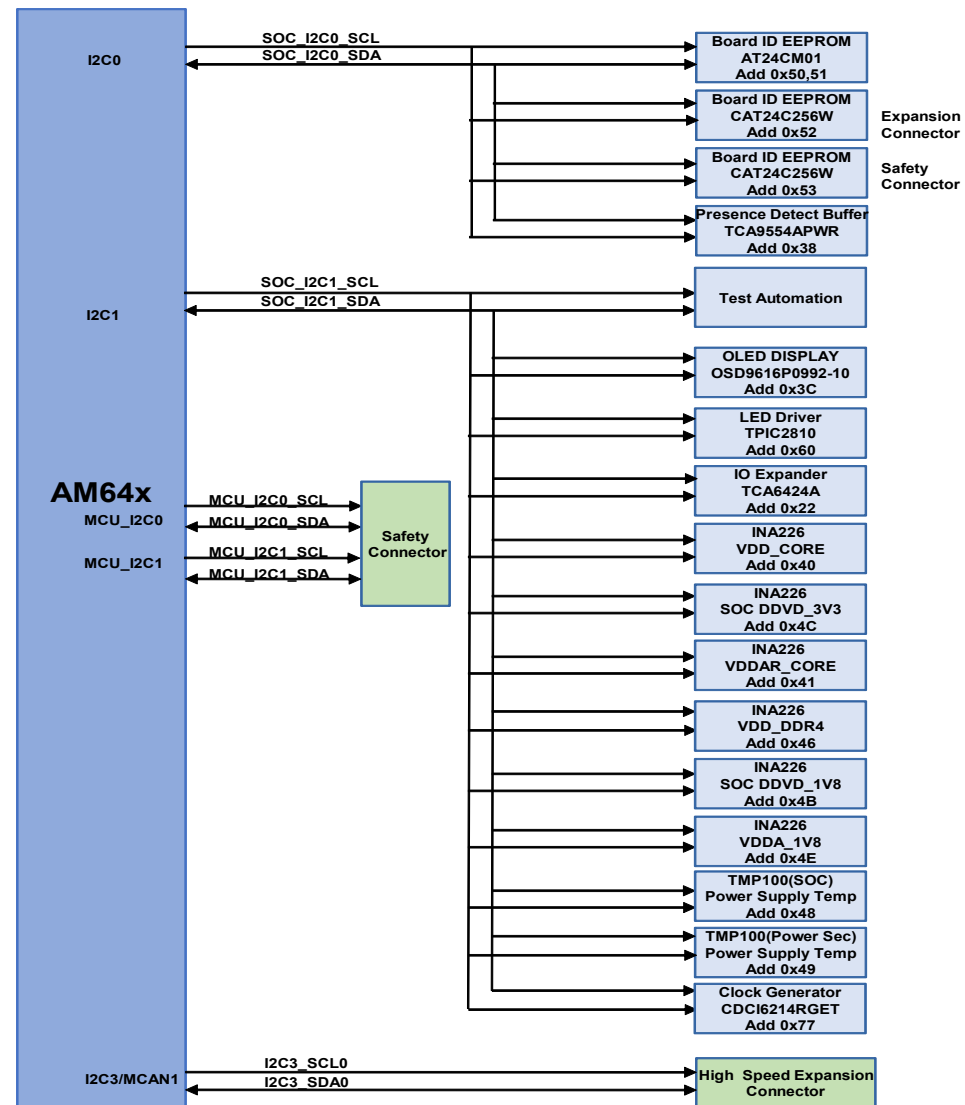
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Title GPIO MAPPING TABLE

Size	Variant Name = PROC101C(002) TMD5243GPEVM	Rev
C		E2
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I2C TREE



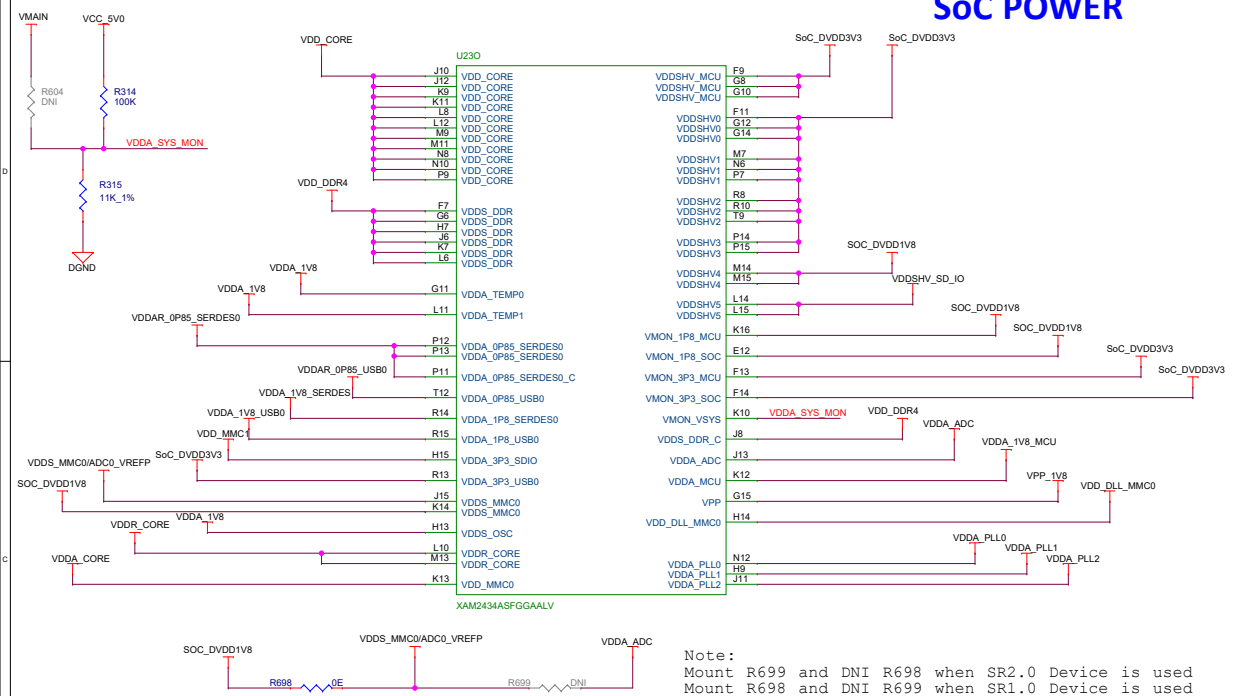
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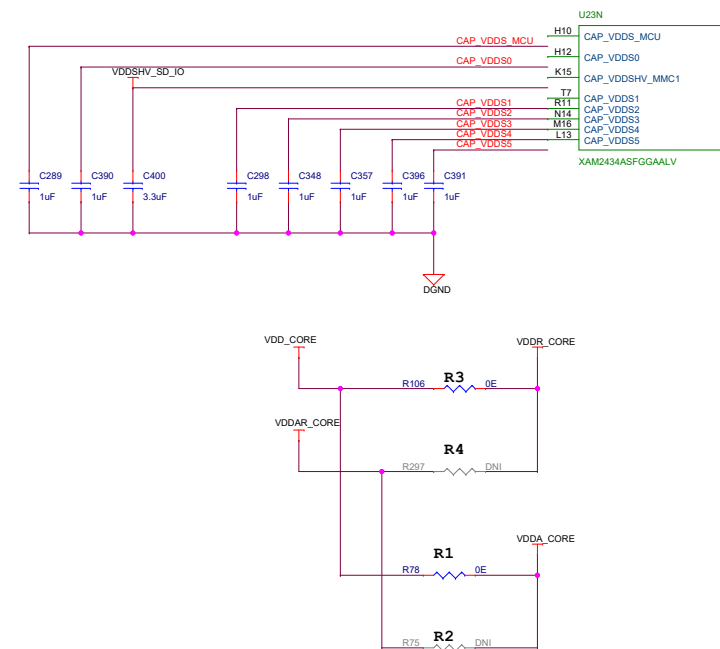
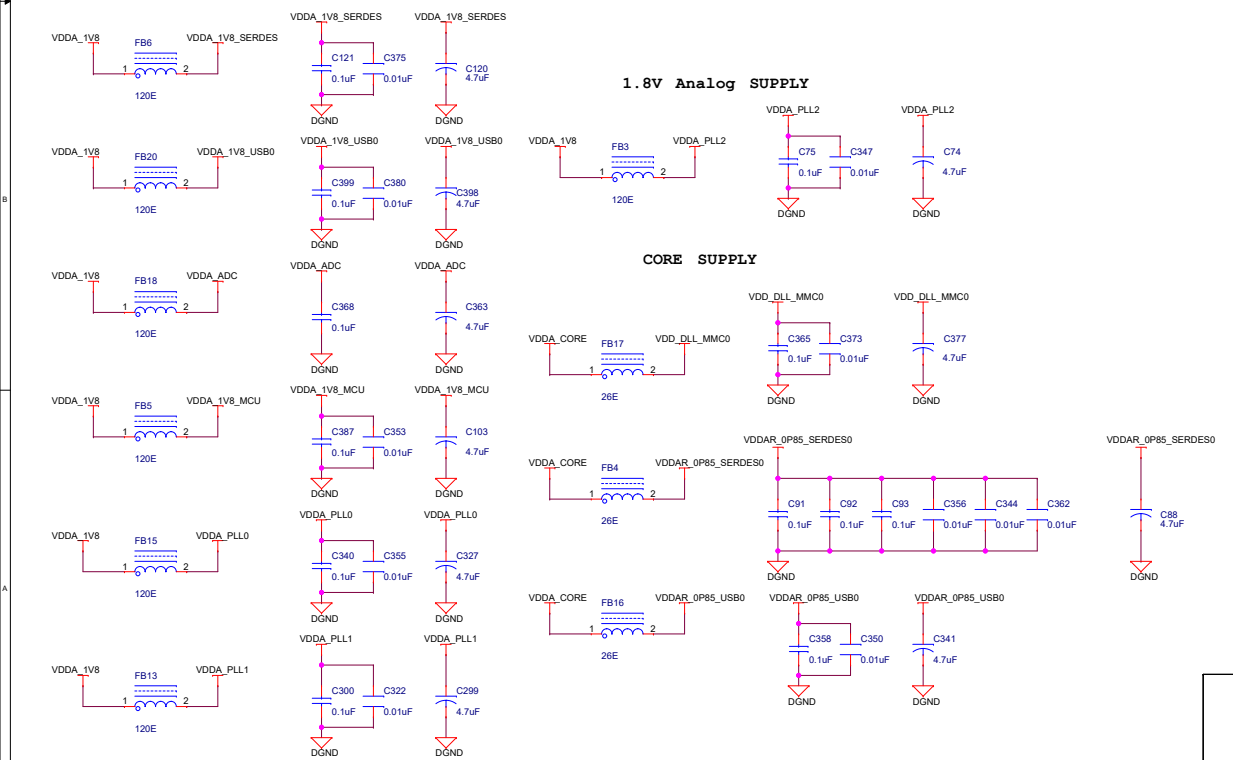
Title I2C TREE

Size	Variant Name = PROC101C(002) TMD5243GPEVM	Rev
C		E2
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SoC POWER



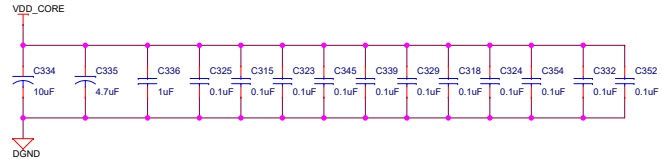
1.8V Analog SUPPLY



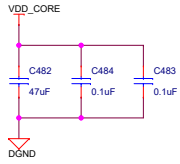
CORE SUPPLY	ARRAY CORE SUPPLY	STEERING RESISTORS
0.75 VDD_CORE	0.85 VDDR_CORE&OTHERS	R2 & R4 INSTALLED
0.8 VDD_CORE	0.85 VDDR_CORE&OTHERS	R2 & R4 INSTALLED
0.8 VDD_CORE & OTHERS	0.85 VDDR_CORE	R1 & R4 INSTALLED
0.85 VDD_CORE,VDDR_CORE&OTHERS	NONE	R1 & R3 INSTALLED



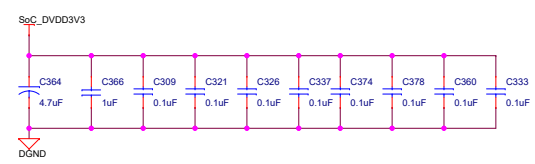
SoC POWER Decaps



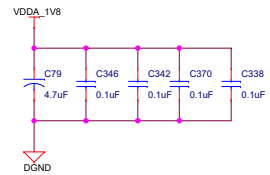
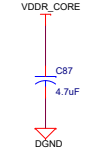
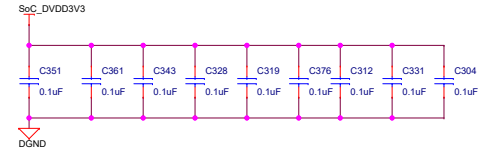
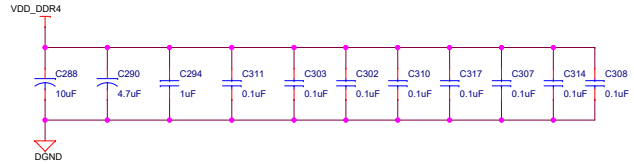
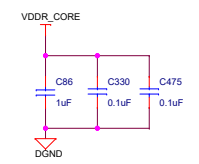
Place one 0.1uF cap near each Pin



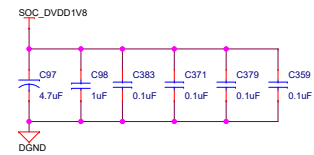
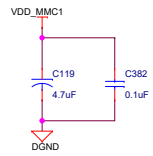
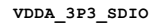
To place after current sense
resistor on VDD_CORE plane



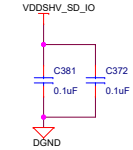
Place one 0.1uF cap near each Pin



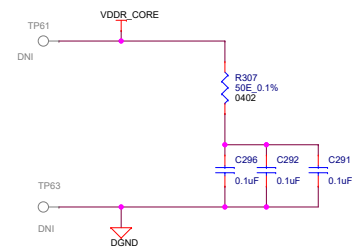
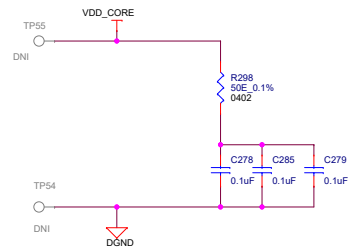
Place one 0.1uF cap near each Pin



Place one 0.1uF cap near each Pin



Core & Array Core Supply Kelvin Sensing



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Title	SOC POWER CAPS
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Size
C

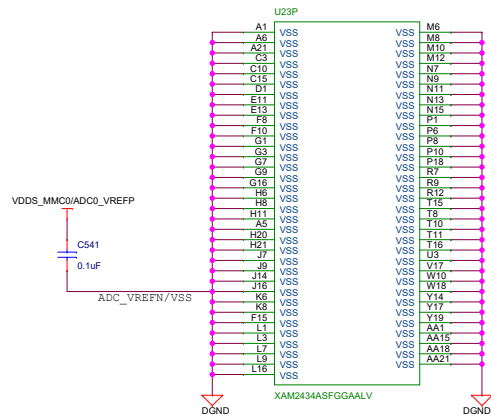
Variant Name = PROC101C(002) TMDS243GPEVM

Rev
E2

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SoC POWER - VSS

CAD Note:
Place CAP C541
between pins
J15 and J16



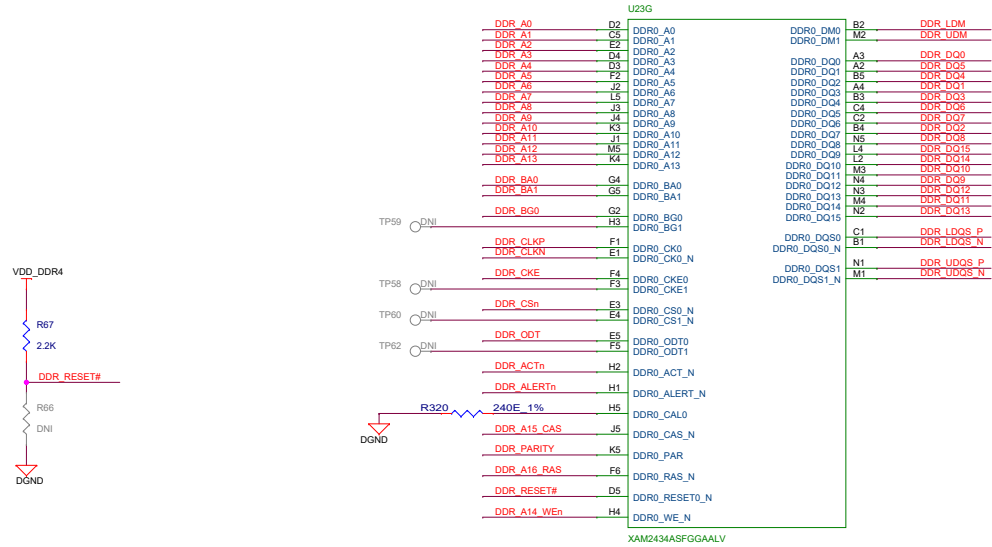
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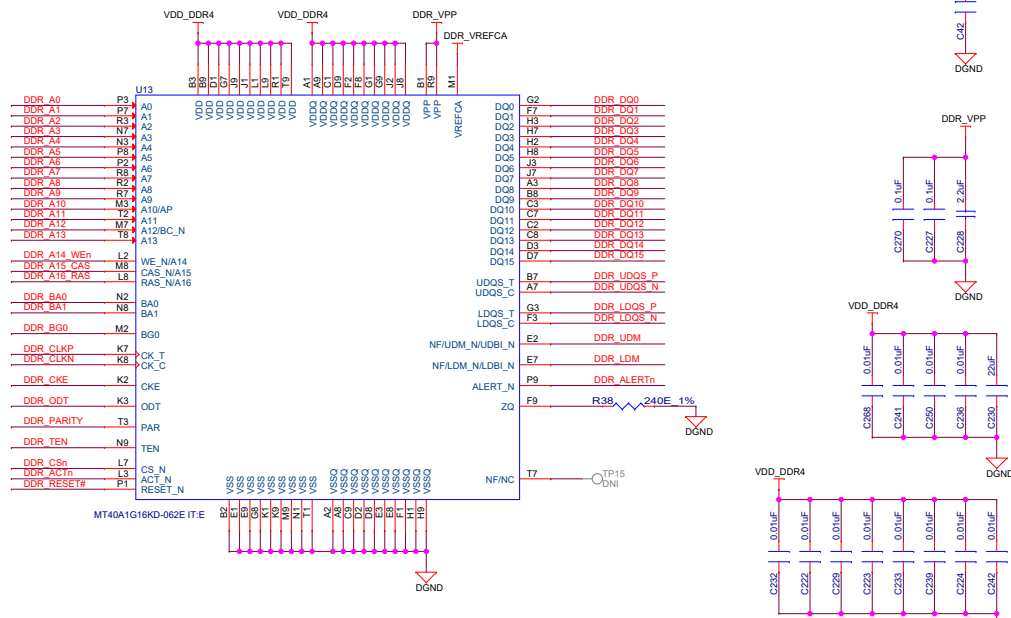
Title SOC VSS

Size	Variant Name = PROC101C(002) TMD5243GPEVM	Rev
C		E2
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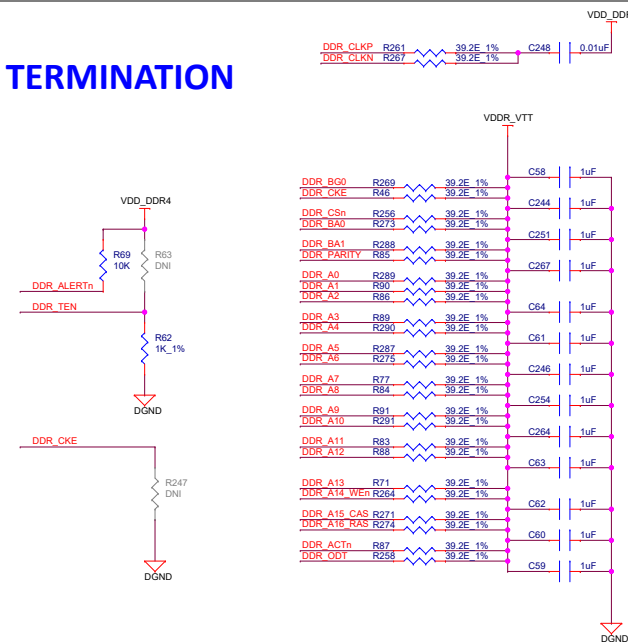
SoC DDR INTERFACE



DDR4 DEVICE



DDR TERMINATION



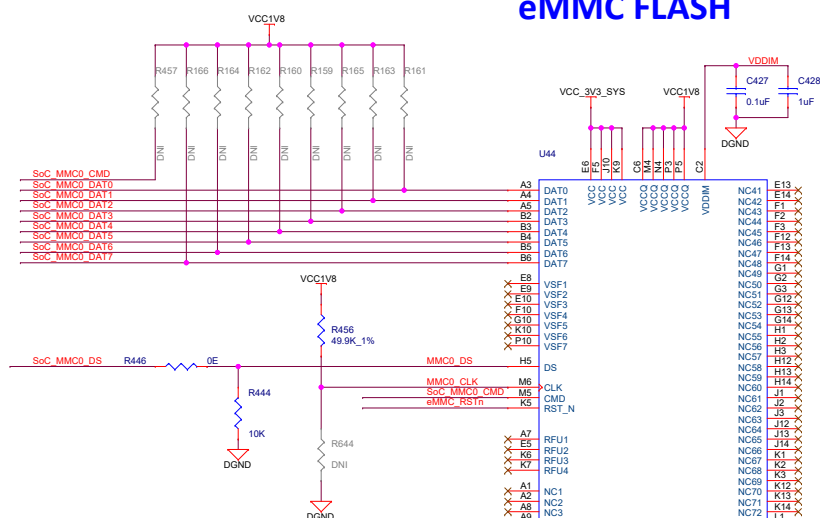
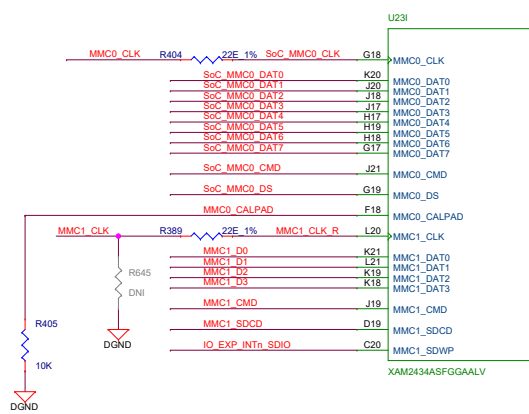
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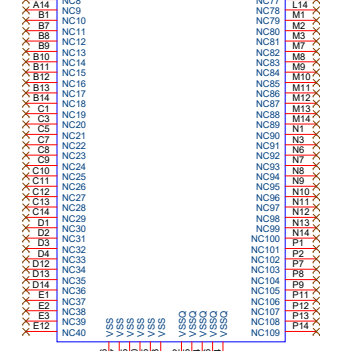
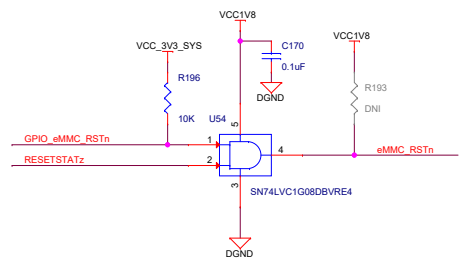
Title DDR INTERFACE

Size	Variant Name = PROC101C(002) TMD5243GPEVM	Rev
C		E2
Date:	Monday, August 22, 2022	Sheet 12 of 40

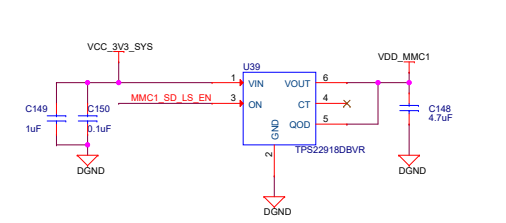
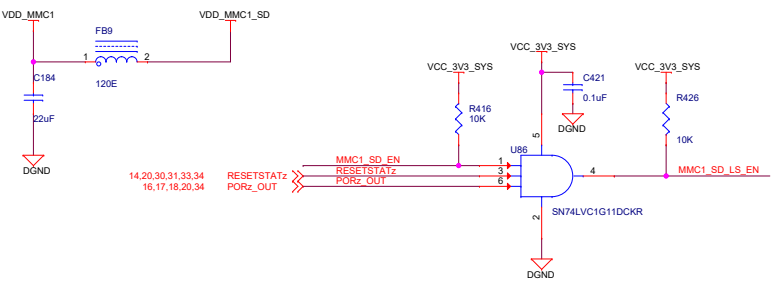
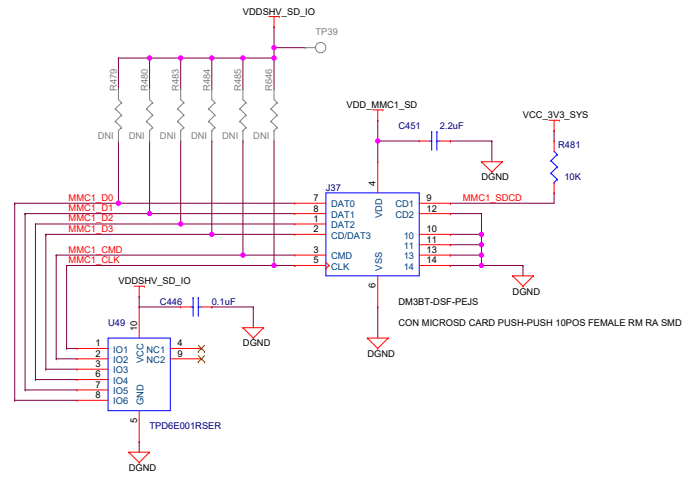
eMMC FLASH



eMMC FLASH RESET



SD CARD INTERFACE



Off Page Connections

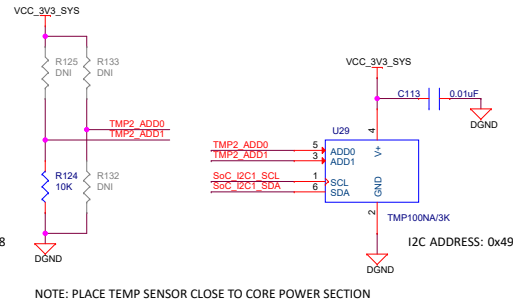
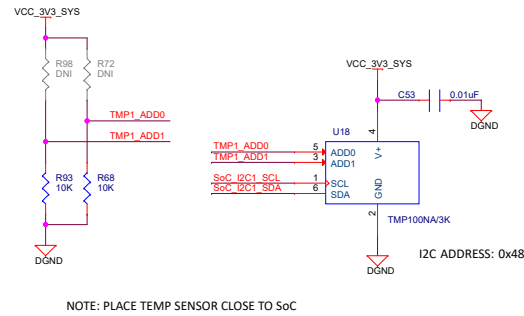
From 4	IO_EXP_INTn_SDIO	IO_EXP_INTn_SDIO
To IO Expander	GPIO_eMMC_RSTn	GPIO_eMMC_RSTn
	MMC1_SD_EN	MMC1_SD_EN

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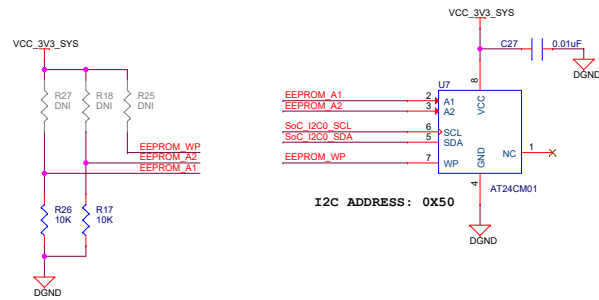
Title		eMMC FLASH_SDCARD INTERFACE	
Size	C	Variant Name = PROC101C(002) TMD5243GPEVM	Rev E2
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TEMPERATURE SENSOR

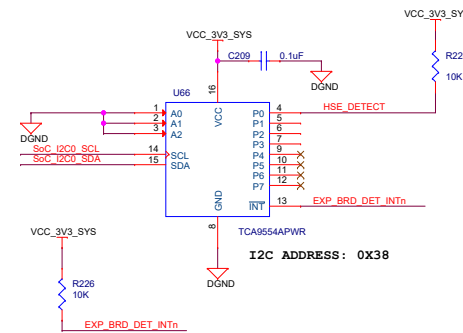


SoC I2C1 SCL DNI TP25
SoC I2C1 SDA DNI TP27

BOARD ID EEPROM



BOARD PRESENCE DETECT CIRCUIT



Off Page Connections

HSE_DETECT	←	HSE_DETECT	27
SoC I2C1 SDA	↔	SoC I2C1 SDA	19,21,29,30,31,32,33
SoC I2C1 SCL	↔	SoC I2C1 SCL	19,21,29,30,31,32,33
SoC I2C0 SDA	↔	SoC I2C0 SDA	27,29,33
SoC I2C0 SCL	↔	SoC I2C0 SCL	27,29,33

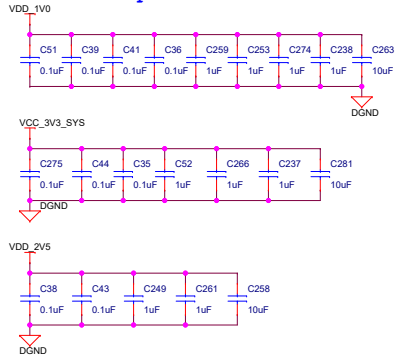
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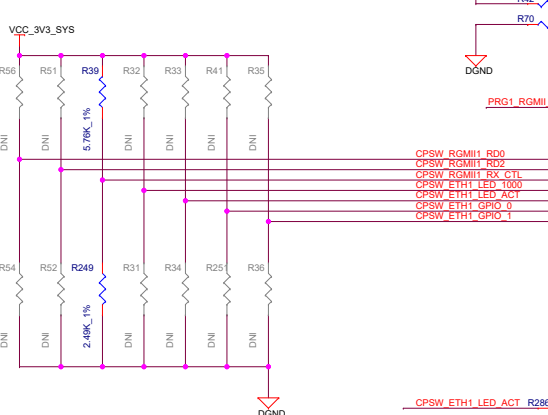
Title EEPROM, PRESENCE DETECTION & TEMP SENSOR

Size	Variant Name = PROC101C(002) TMD5243GPEVM	Rev
C		E2
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Decaps

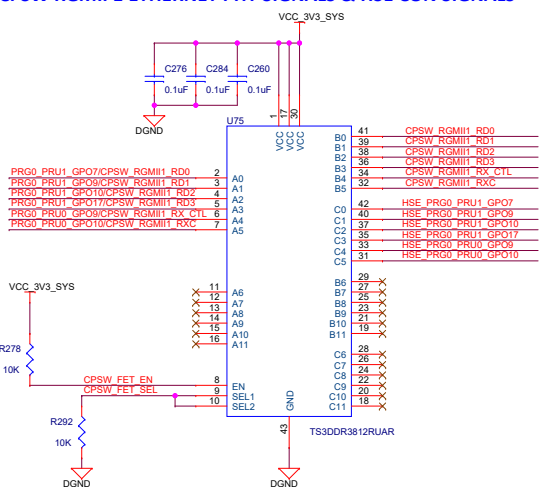


STRAPPING RESISTORS

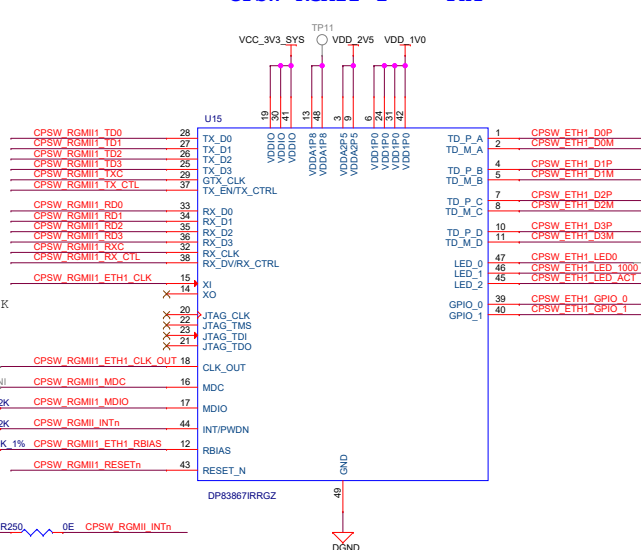


```
PHY ADDRESS = 00000
Auto-negotiation Enabled
10/100/1000 advertised, Auto-MDI-X
Tx & Rx Clock Skew = 2.0ns
```

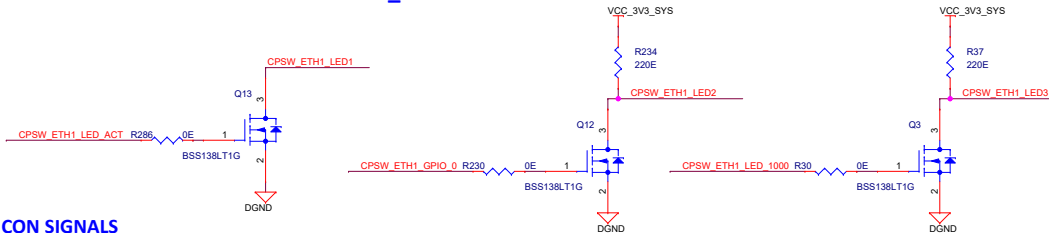
CPSW RGMII 1 ETHERNET PHY SIGNALS & HSE CON SIGNALS



CPSW RGMII 1 - PHY



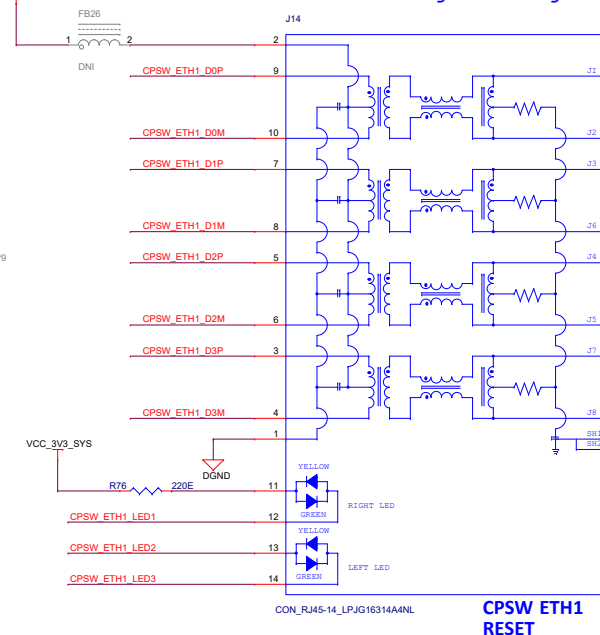
CPSW_ETHERNET PHY- 1 SPEED & ACTIVITY LED 's DRIVERS



TS3DDR3812RUAR Truth Table

EN	SEL1	SEL2	FUNCTION
L	X	X	A0 to A11, B0 to B11, and C0 to C11 are Hi-Z
H	L	L	A0 to A5 = B0 to B5 and A6 to A11 = B6 to B11
H	L	H	A0 to A5 = B0 to B5 and A6 to A11 = C6 to C11
H	H	L	A0 to A5 = C0 to C5 and A6 to A11 = B6 to B11
H	H	H	A0 to A5 = C0 to C5 and A6 to A11 = C6 to C11

RJ45 with Integrated Magnetics



Off Page Connections

```

From  

Processor#7      PRG0_PRU1_GPO7/CPSW_RGMII_RD0 >> PRG0_PRU1_GPO7/CPSW_RGMII_RD0  

    27             PRG0_PRU1_GPO9/CPSW_RGMII_RD1 >> PRG0_PRU1_GPO9/CPSW_RGMII_RD1  

    27             PRG0_PRU1_GPD0/CPSW_RGMII RD2 >> PRG0_PRU1_GPD0/CPSW_RGMII RD2  

    27             PRG0_PRU1_GPD17/CPSW_RGMII RD3 >> PRG0_PRU1_GPD17/CPSW_RGMII RD3  

    27             PRG0_PRU0_CPSW0/RGMII_RX_CTL >> PRG0_PRU0_CPSW0/RGMII_RX_CTL  

    27             PRG0_PRU0_GPD10/CPSW_RGMII_RXC >> PRG0_PRU0_GPD10/CPSW_RGMII_RXC  
  

From Processor          27     CPSW_RGMII_TD0 >> CPSW_RGMII_TD0  

                                27     CPSW_RGMII_TD1 >> CPSW_RGMII_TD1  

                                27     CPSW_RGMII_TD2 >> CPSW_RGMII_TD2  

                                27     CPSW_RGMII_TD3 >> CPSW_RGMII_TD3  

                                27     CPSW_RGMII_TX_CTL >> CPSW_RGMII_TX_CTL  

                                27     CPSW_RGMII_1XC >> CPSW_RGMII_1XC  
  

                                13,17,18,20,34   PORz_OUT >> PORz_OUT  

                                17,18,34       PRG1_RGMII_INTRn >> PRG1_RGMII_INTRn  
  

From IO Expander        16,33  GPIO_CSPW1_RST >> GPIO_CSPW1_RST  

                                33         CPWS_FET_SEL >> CPWS_FET_SEL  
  

From Clock Buffer        31     CPSW_RGMII1_ETH1_CLK >> CPSW_RGMII1_ETH1_CLK  
  

To HSE Connector        27     HSE_PRG0_PRU1_GPO7 >> HSE_PRG0_PRU1_GPO7  

                                27     HSE_PRG0_PRU1_GPO9 >> HSE_PRG0_PRU1_GPO9  

                                27     HSE_PRG0_PRU1_GPD0 >> HSE_PRG0_PRU1_GPD0  

                                27     HSE_PRG0_PRU1_GPD17 >> HSE_PRG0_PRU1_GPD17  

                                27     HSE_PRG0_PRU0_GPO9 >> HSE_PRG0_PRU0_GPO9  

                                27     HSE_PRG0_PRU0_GPD10 >> HSE_PRG0_PRU0_GPD10  
  

From Processor          17,27  CPSW_RGMII_MDIO <<< CPSW_RGMII1_MDIO  

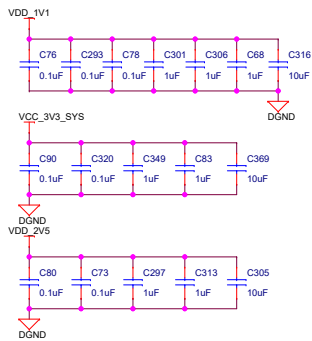
                                17,27  CPSW_RGMII_MDC <<< CPSW_RGMII1_MDC

```

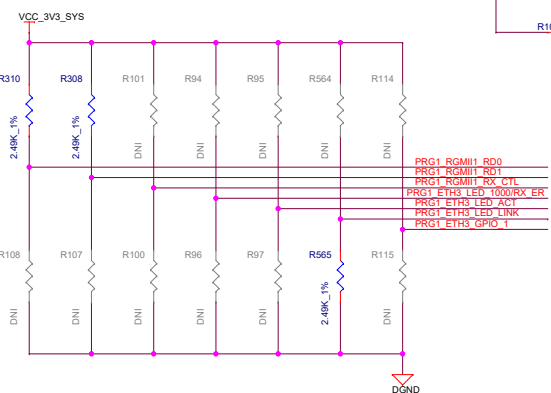

Size	Variant Name = PROC101C(002) TMDS243GPEVM	
C		
Date:	Monday, August 22, 2022	Sheet 17 of 40

ICSSG1 - RGMII 1

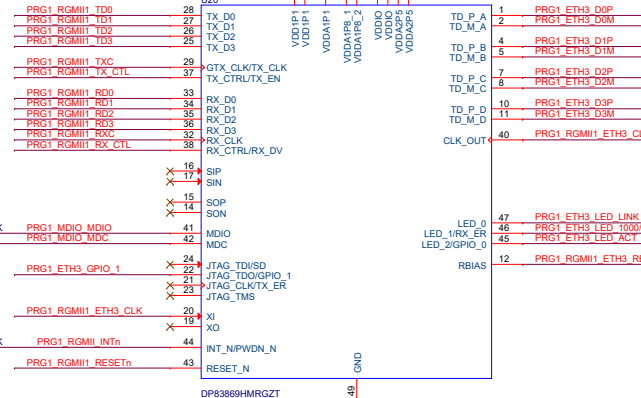
Decaps



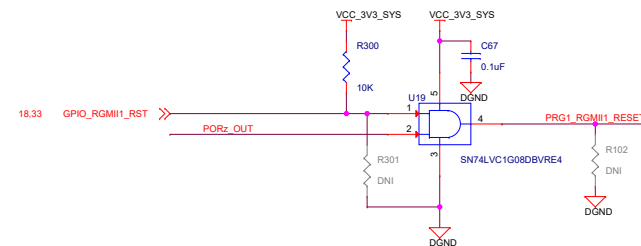
STRAPPING RESISTORS



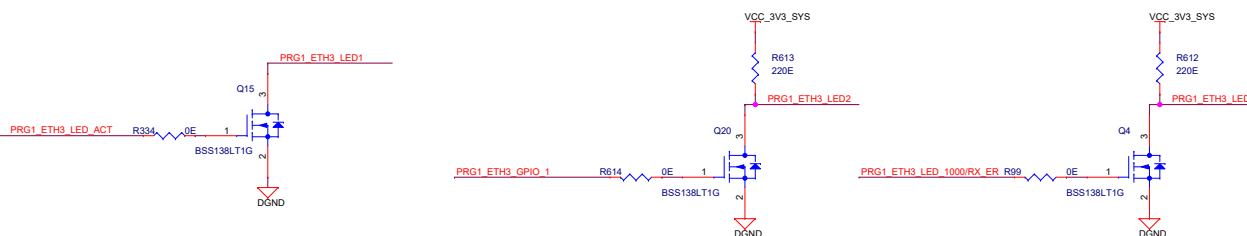
PHY ADDRESS = 01111
Auto-negotiation, 10/100/1000 advertised, Auto-MDI-X
RGMII to Copper (1000Base-TX/10Base-T)



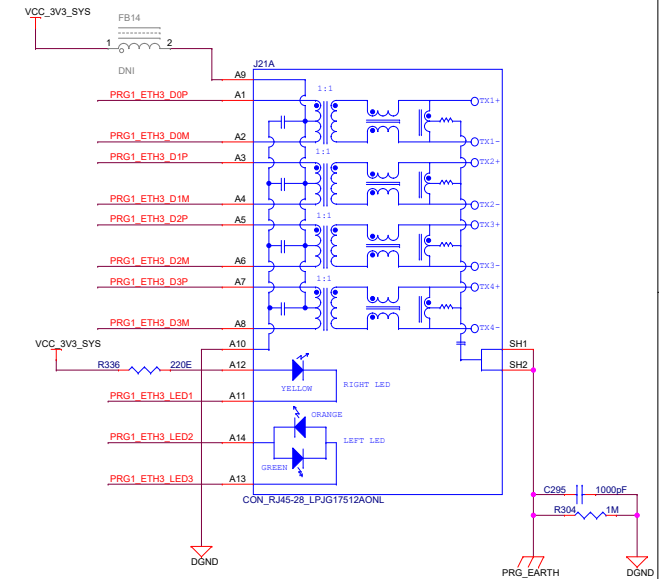
PRG1 ETH2 RESET



PRG1_ETHERNET - 3 SPEED & ACTIVITY LED's DRIVERS



Dual RJ45 CON With Integrated Magnetics



Off Page Connections

To Processor	16,17,34	PRG1_RGMII_INTn	PRG1_RGMII_INTn
	27	PRG1_RGMII_RD0	PRG1_RGMII_RD0
	27	PRG1_RGMII_RD1	PRG1_RGMII_RD1
	27	PRG1_RGMII_RD2	PRG1_RGMII_RD2
	27	PRG1_RGMII_RD3	PRG1_RGMII_RD3
	27	PRG1_RGMII_RXC	PRG1_RGMII_RXC
	27	PRG1_RGMII_RX_CTL	PRG1_RGMII_RX_CTL
13,16,17,20,34	PORz_OUT	PORz_OUT	
	27	PRG1_ETH3_LED_LINK	PRG1_ETH3_LED_LINK
27	PRG1_ETH3_LED_1000RX_ER	PRG1_ETH3_LED_1000RX_ER	
From Processor	27	PRG1_RGMII_TD0	PRG1_RGMII_TD0
	27	PRG1_RGMII_TD1	PRG1_RGMII_TD1
	27	PRG1_RGMII_TD2	PRG1_RGMII_TD2
	27	PRG1_RGMII_TD3	PRG1_RGMII_TD3
	27	PRG1_RGMII_TXC	PRG1_RGMII_TXC
	27	PRG1_RGMII_TX_CTL	PRG1_RGMII_TX_CTL
	31	PRG1_RGMII_ETH3_CLK	PRG1_RGMII_ETH3_CLK
From Processor	17,27	PRG1_MDIO_MDIO	PRG1_MDIO_MDIO
	17,27	PRG1_MDIO_MDC	PRG1_MDIO_MDC
From IO Expander	18,33	GPIO_RGMII_RST	GPIO_RGMII_RST
	31	PRG1_RGMII_ETH3_CLK	PRG1_RGMII_ETH3_CLK

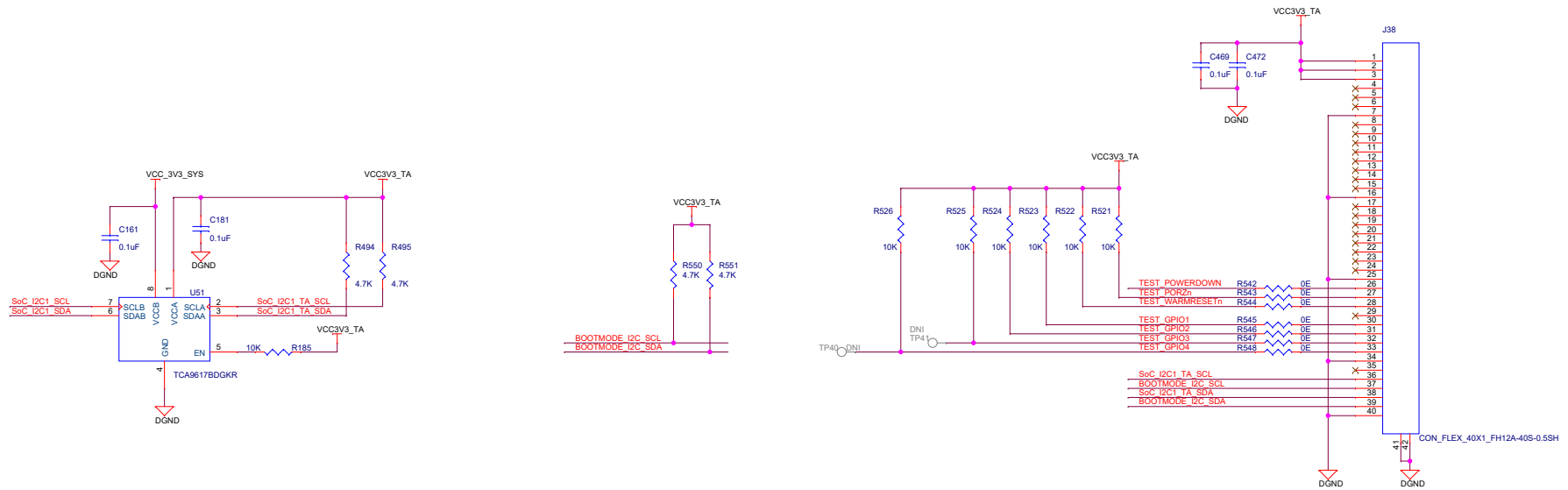
Designed for TI by Mistral Solutions Pvt Ltd



Title		ICSSG2 RGMII_1 ETHERNET PHY	
Size	Variant Name = PROC101C(002) TMD5243GPEVM	Rev	
C		E2	
Date:	Monday, August 22, 2022	Sheet	18 of 40

TEST AUTOMATION

40-PIN AUTOMATION HEADER



TEST AUTOMATION GPIO MAPPING

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TEST_POWERDOWN	Used to Power down the OVP Circuit	OUTPUT	External Pullup
TEST_PORZn	Used to Reset the SoC PORz	OUTPUT	External Pullup
TEST_WARMRESETn	Used to Reset the SoC Warmreset	OUTPUT	External Pullup
TEST_GPIO1	Used to Generate the interrupt on GPIO0_13_INTn Pin	OUTPUT	External Pullup
TEST_GPIO2	Connected to I/O Expander to Communicate with SoC	OUTPUT	External Pullup
TEST_GPIO3	Used to Enable the BOOTMODE Buffer	OUTPUT	External Pullup
TEST_GPIO4	Used to Reset the Bootmode IO Expander	OUTPUT	External Pullup

Off Page Connections

To Processor	15,21,29,30,31,32,33	SoC_I2C1_SCL	SoC_I2C1_SCL
	15,21,29,30,31,32,33	SoC_I2C1_SDA	SoC_I2C1_SDA
To Bootmode Buffer	20	BOOTMODE_I2C_SCL	BOOTMODE_I2C_SCL
	20	BOOTMODE_I2C_SDA	BOOTMODE_I2C_SDA
To Debounce Ckt	35	TEST_PORZn	TEST_PORZn
To High Side SW	37	TEST_POWERDOWN	TEST_POWERDOWN
To Debounce Ckt	35	TEST_WARMRESETn	TEST_WARMRESETn
To IO Expander	35	TEST_GPIO1	TEST_GPIO1
To EN Boot Mode Buffer	33	TEST_GPIO2	TEST_GPIO2
To RST Boot Mode Buffer	20	TEST_GPIO3	TEST_GPIO3
	20	TEST_GPIO4	TEST_GPIO4

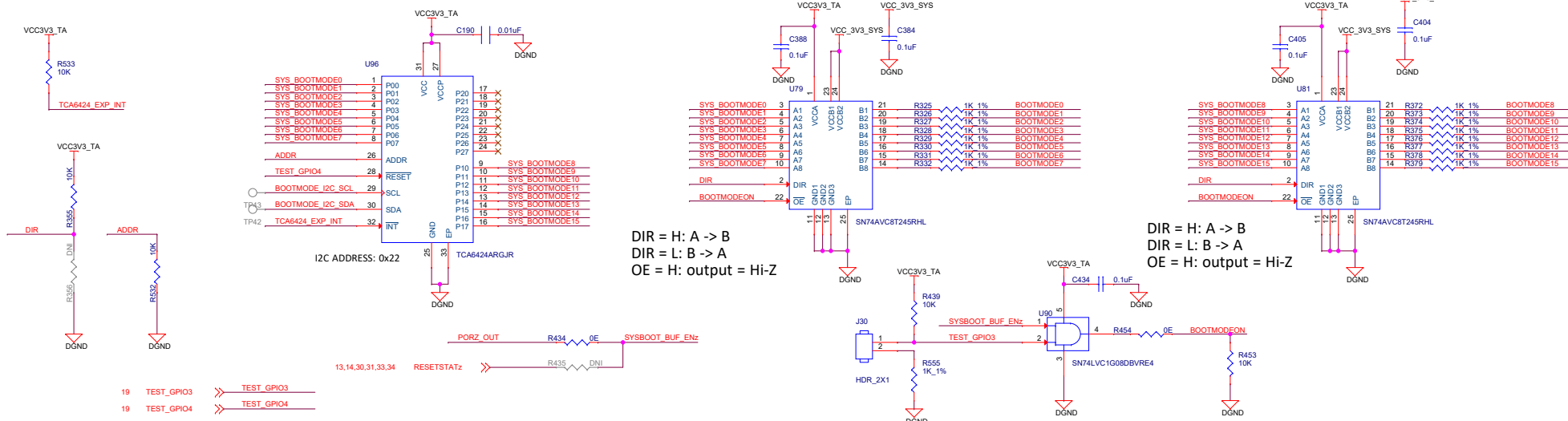
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Title TEST AUTOMATION

Size	Variant Name = PROC101C(002) TMD5243GPEVM	Rev
C		E2
Date:	Monday, August 22, 2022	Sheet 19 of 40

BOOT MODE BUFFER & SWITCHES



DIR = H: A -> B
 DIR = L: B -> A
 OE = H: output = Hi-Z

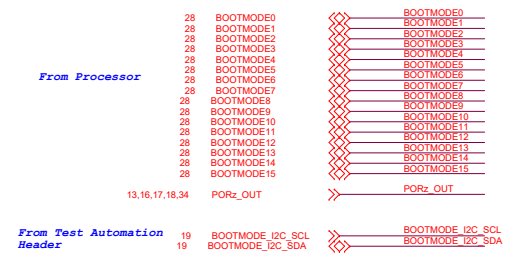
DIR = H: A -> B
 DIR = L: B -> A
 OE = H: output = Hi-Z

SWITCH ON = LOGIC 1
 SWITCH OFF = LOGIC 0

BOOT MODES SUPPORTED

1. OSPI
2. MMC1 - SD CARD
3. MMC0 - eMMC
4. CPSW Ethernet Slave
5. USB Host
6. USB Device
7. UART
8. Ethernet

Off Page Connections



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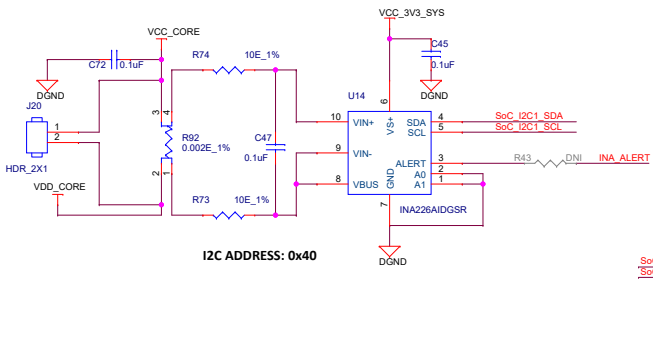


Title BOOT MODE BUFFER & SWITCHES

Size	Variant Name = PROC101C(002) TMD5243GPEVM	Rev
C		E2
Date:	Monday, August 22, 2022	Sheet 20 of 40

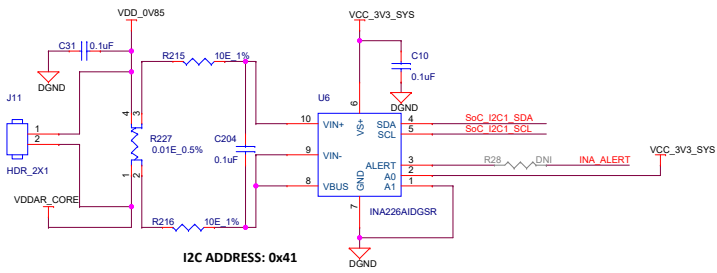
CURRENT MONITORING DEVICES

VDD_CORE



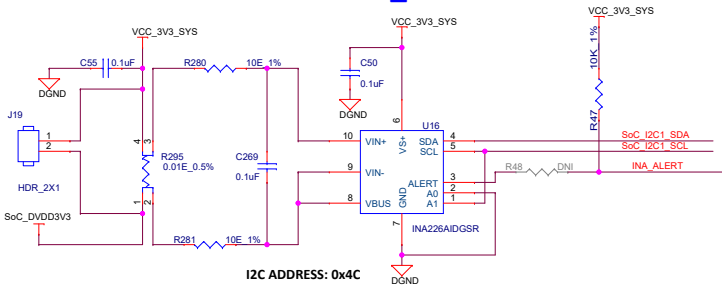
I2C ADDRESS: 0x40

VDDAR_CORE

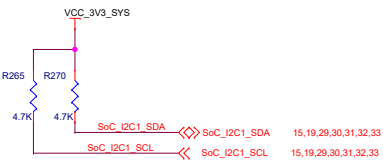


I2C ADDRESS: 0x41

SoC_DVDD3V3



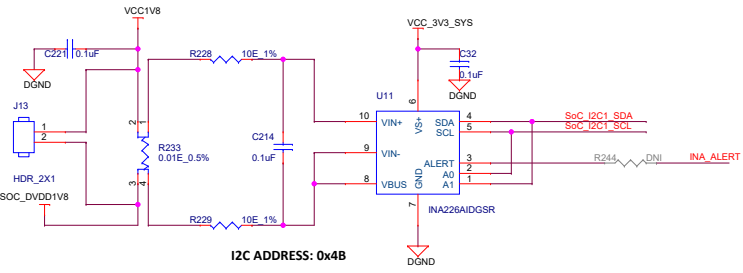
I2C ADDRESS: 0x4C



SoC_I2C1_SDA
SoC_I2C1_SCL

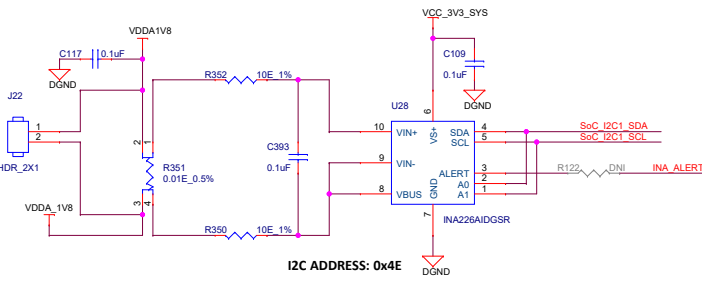
15, 19, 29, 30, 31, 32, 33
15, 19, 29, 30, 31, 32, 33

SoC_DVDD1V8



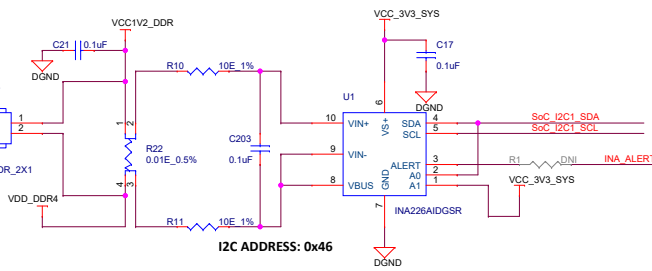
I2C ADDRESS: 0x4B

VDDA_1V8



I2C ADDRESS: 0x4E

VDD_DDR4



I2C ADDRESS: 0x46

INA I2C SLAVE ADDRESS		
POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (IN HEX)
VCC_CORE	VDD_CORE	40
VDD_OV85	VDDAR_CORE	41
VCC_3V3_SYS	SoC_DVDD3V3	4C
VCC1V8	SoC_DVDD1V8	4B
VDDA1V8	VDDA_1V8	4E
VCC1V2_DDR	VDD_DDR4	46

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Title CURRENT MONITORING DEVICES

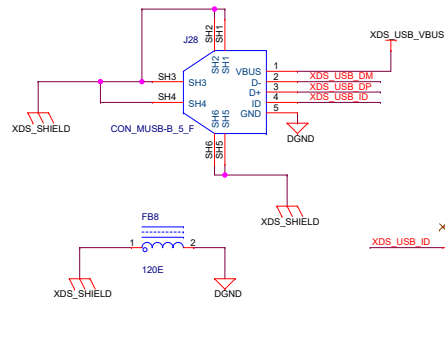
Size Variant Name = PROC101C(002) TMD5243GPEVM

Date: Monday, August 22, 2022

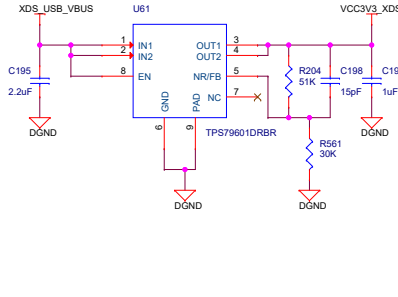
Sheet 21 of 40

Rev E2

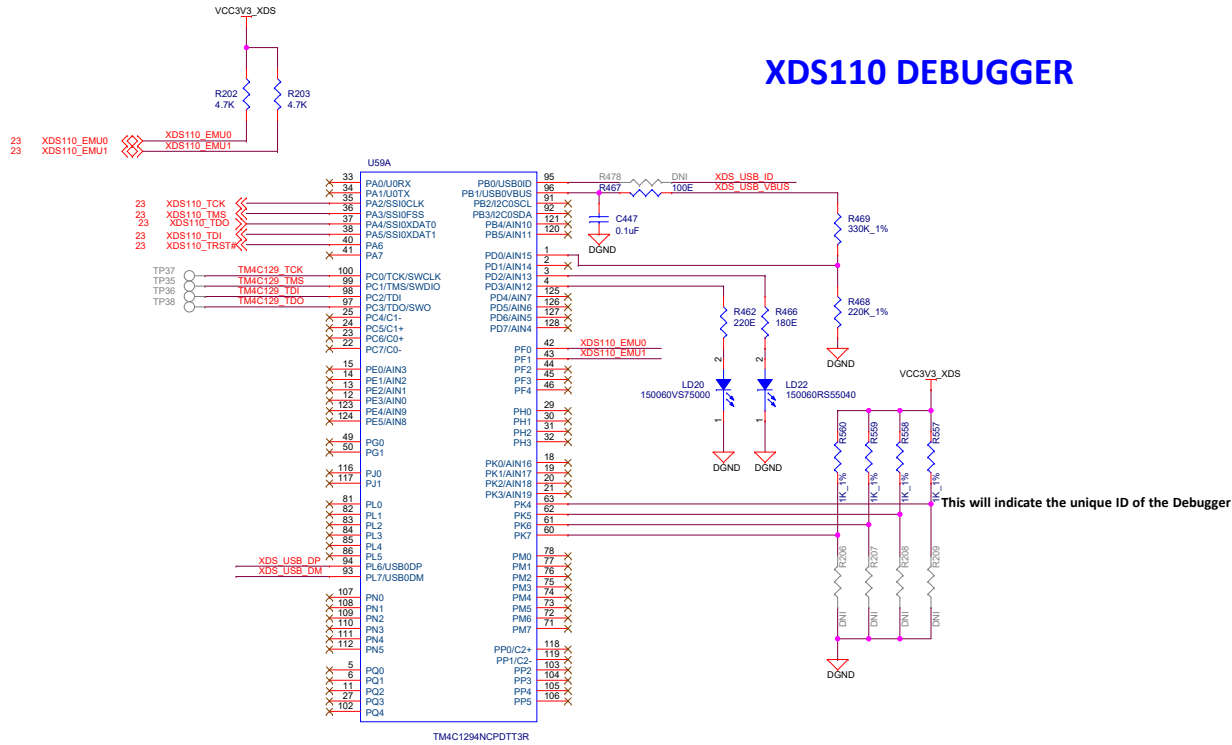
USB Connector



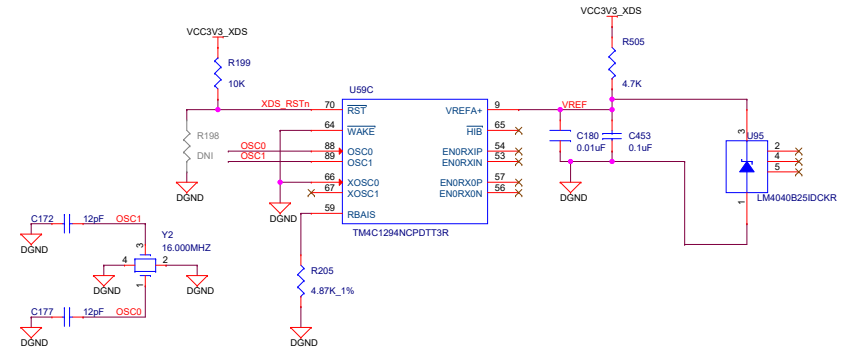
XDS110 POWER



XDS110 DEBUGGER



This will indicate the unique ID of the Debugger



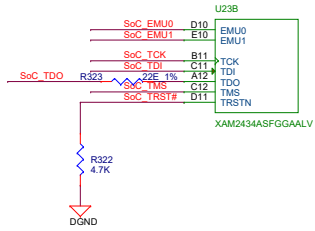
Designed for TI by Mistral Solutions Pvt Ltd



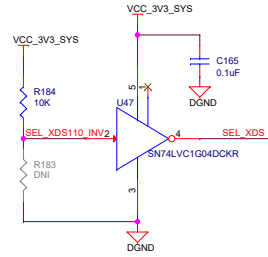
Title XDS110 DEBUGGER

Size	Variant Name = PROC101C(002) TMS3243GPEVM	Rev
C		E2
Date:	Monday, August 22, 2022	Sheet 22 of 40

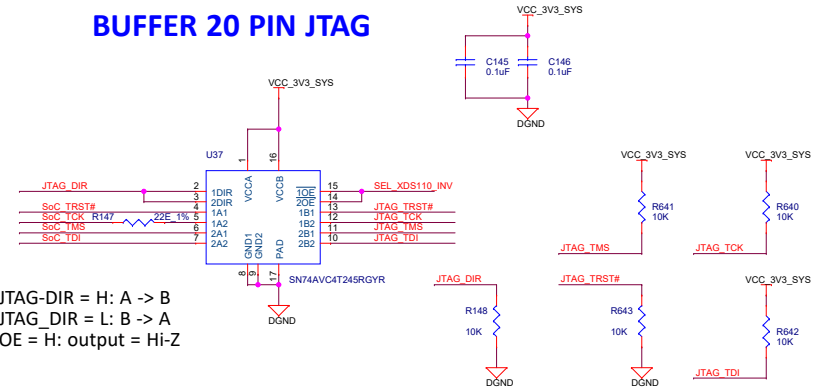
JTAG SoC SECTION



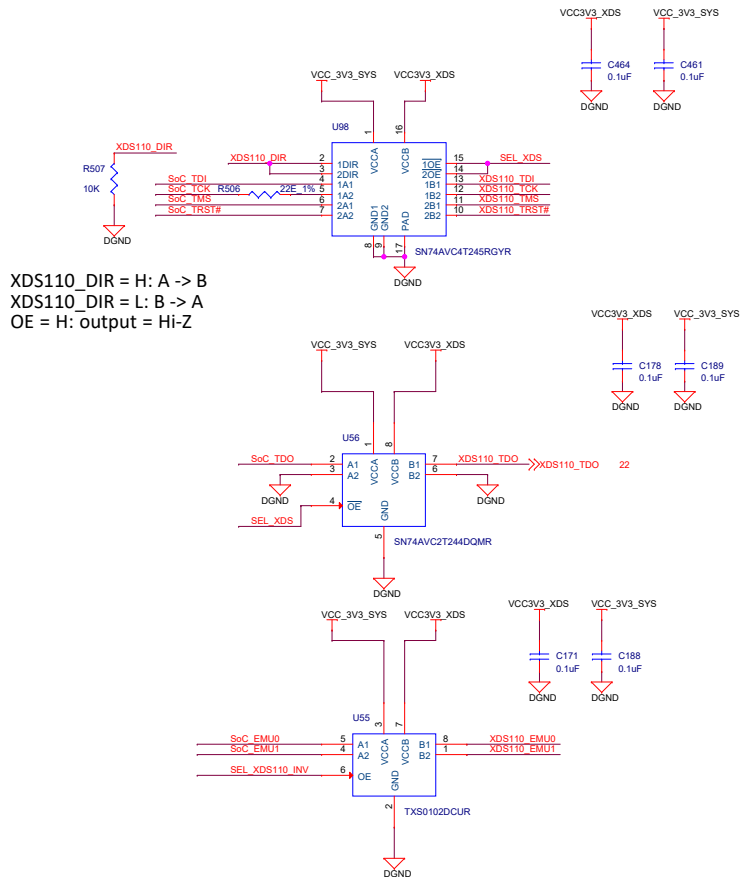
JTAG BUFFER



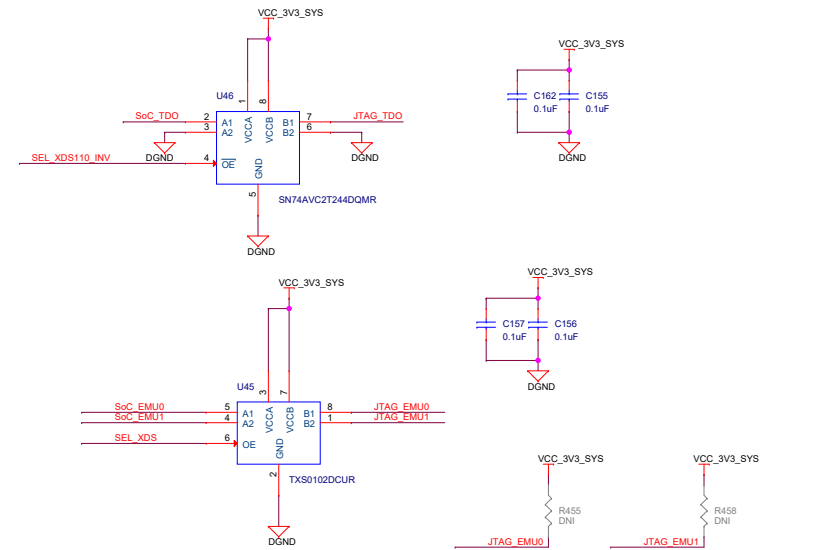
BUFFER 20 PIN JTAG



BUFFER XDS110



Placement of Buffers U37, U46, U56 and U98 to be changed to reduce Stub length of the JTAG signals. These buffers need to be placed closer to the cTI-20pin connector -J25



Off Page Connections

24	SEL_XDS110_INV	JTAG_EMU0
24	JTAG_EMU0	JTAG_EMU1
24	JTAG_EMU1	XDS110_TDI
22	XDS110_TDI	XDS110_TCK
22	XDS110_TCK	XDS110_TMS
22	XDS110_TMS	XDS110_TRST#
22	XDS110_TRST#	JTAG_TDI
24	JTAG_TDI	JTAG_TCK
24	JTAG_TCK	JTAG_TMS
24	JTAG_TMS	JTAG_TRST#
24	JTAG_TRST#	XDS110_EMU0
22	XDS110_EMU0	XDS110_EMU1

From XDS1100 Debugger

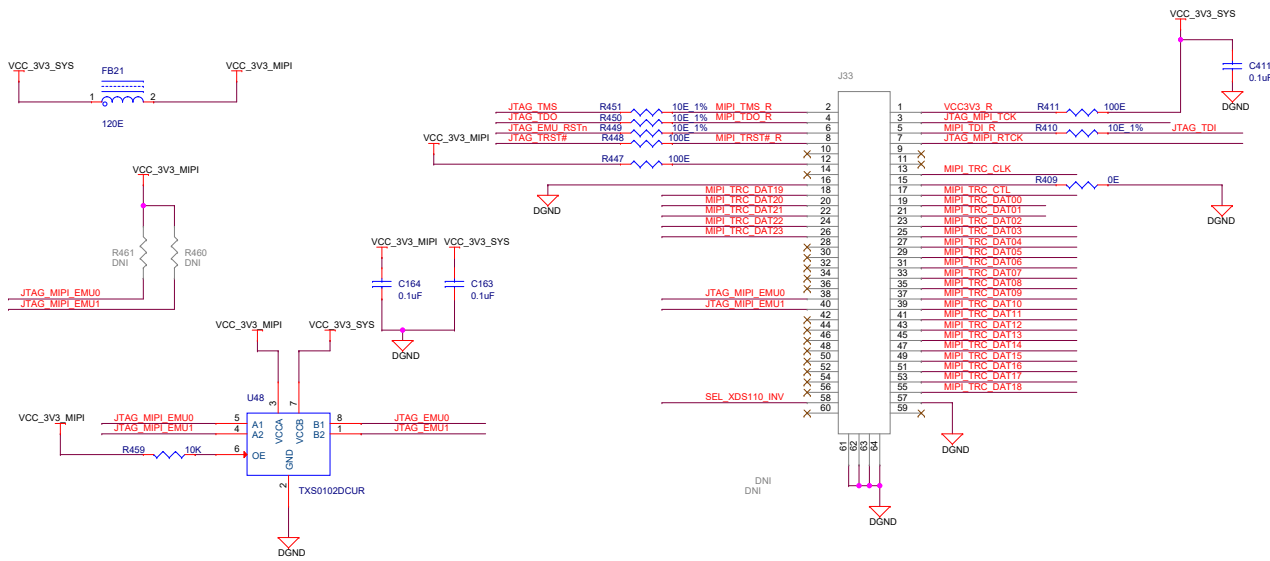
Designed for TI by Mistral Solutions Pvt Ltd



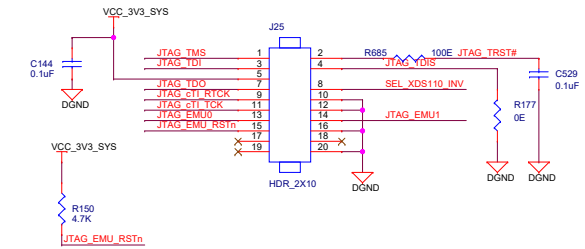
Title JTAG BUFFER

Size	Variant Name = PROC101C(002) TMD5243GPEVM	Rev
C		E2
Date:	Monday, August 22, 2022	Sheet 23 of 40

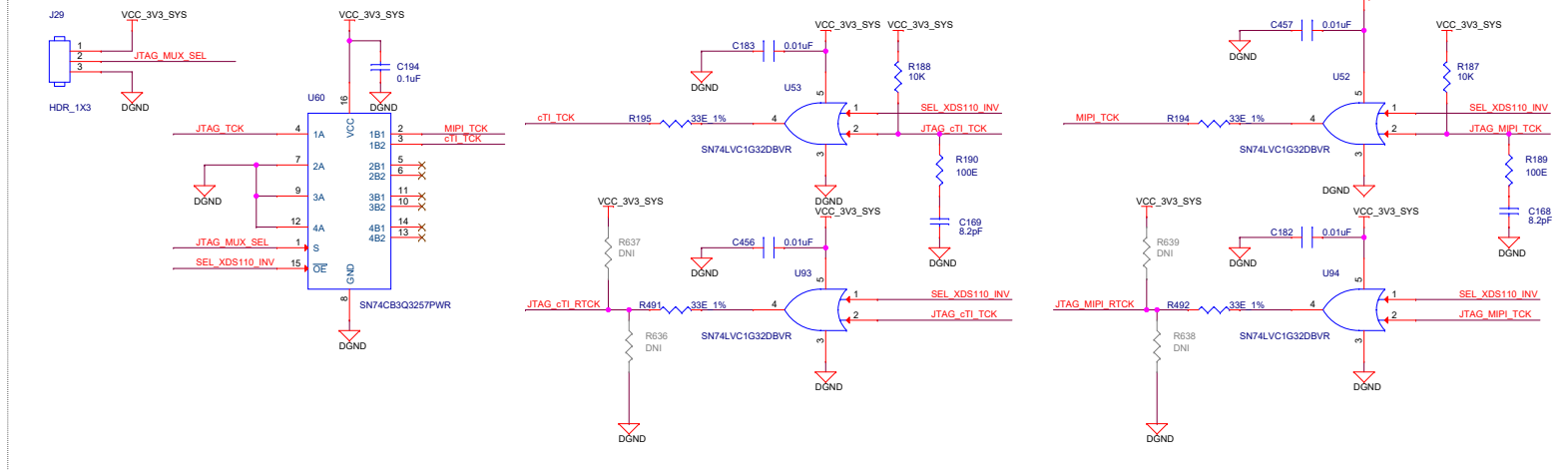
MIPI 60 PIN CONNECTOR



JTAG 20 PIN cTI CONNECTOR



JTAG CLOCK BUFFER

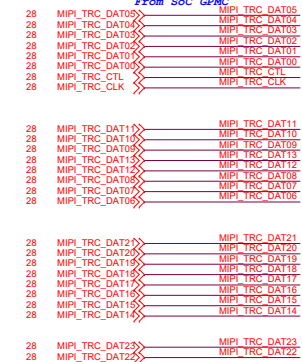


Off Page Connections

From JTAG Buffer



From SoC GPMC

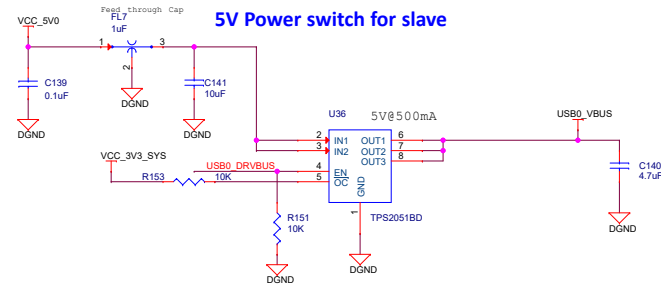
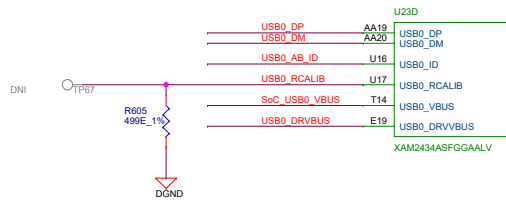


Designed for TI by Mistral Solutions Pvt Ltd

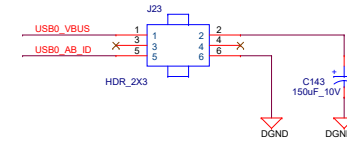


Title				MPII 60 PIN CONNECTOR			
Size		Variant Name = PROC101C(002) TMDS243GPEVM				Rev	
C						E2	
Date:		Monday, August 22, 2022		Sheet		24 of 40	

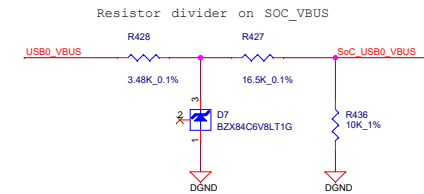
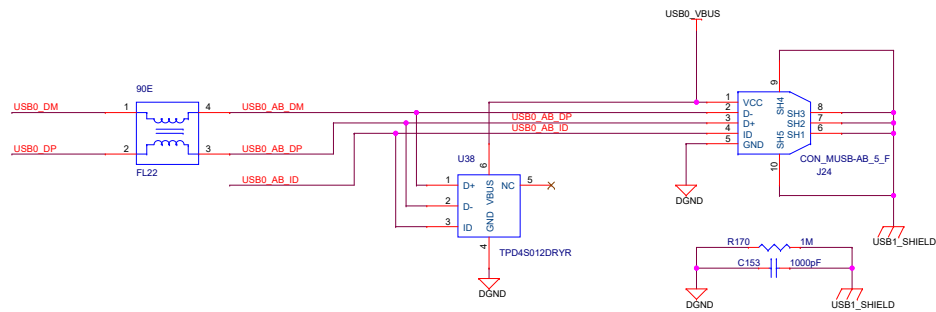
USB 2.0 INTERFACE



2X3 header to enable bulk capacitance on USB0_VBUS in host mode and to ground USB0_AB_ID pin, if a non standard cable is used



Micro USB 2.0 AB Connector



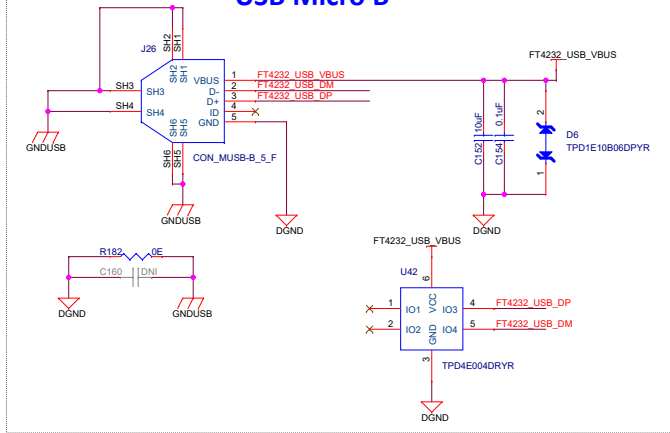
Designed for TI by Mistral Solutions Pvt Ltd



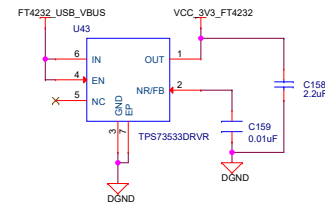
Title USB 2.0 INTERFACE

Size	Variant Name = PROC101C(002) TMD6243GPEVM	Rev
C		E2
Date:	Monday, August 22, 2022	Sheet 25 of 40

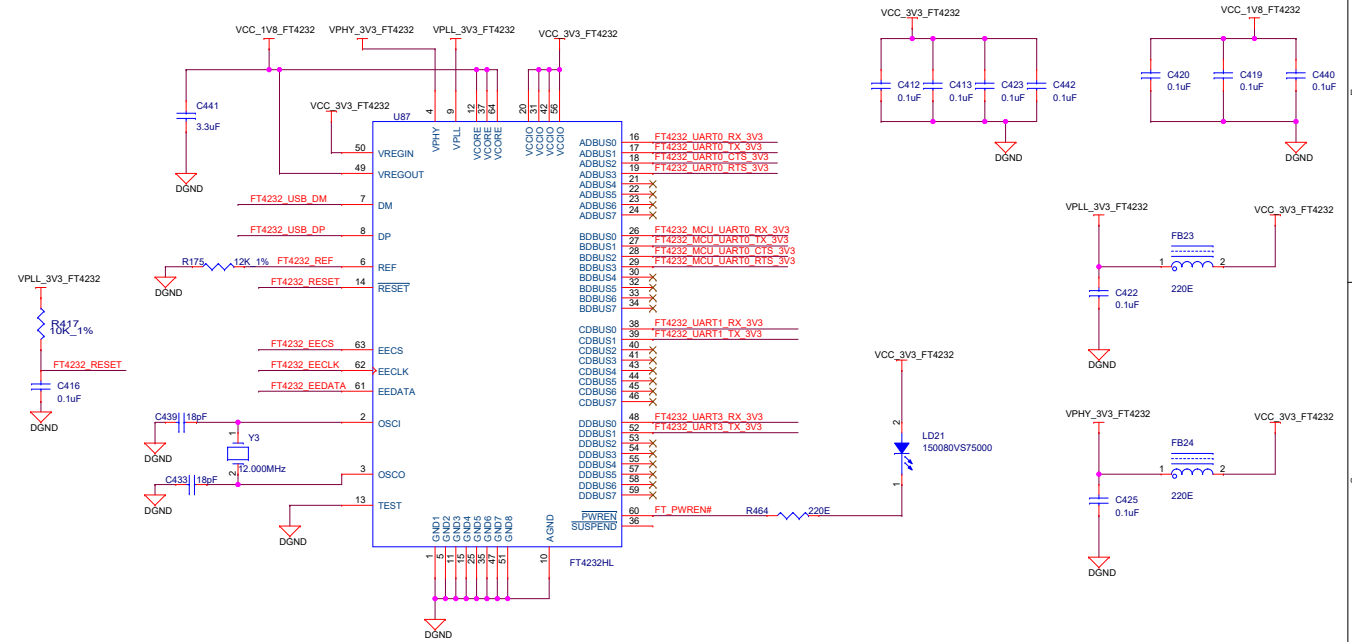
USB Micro B



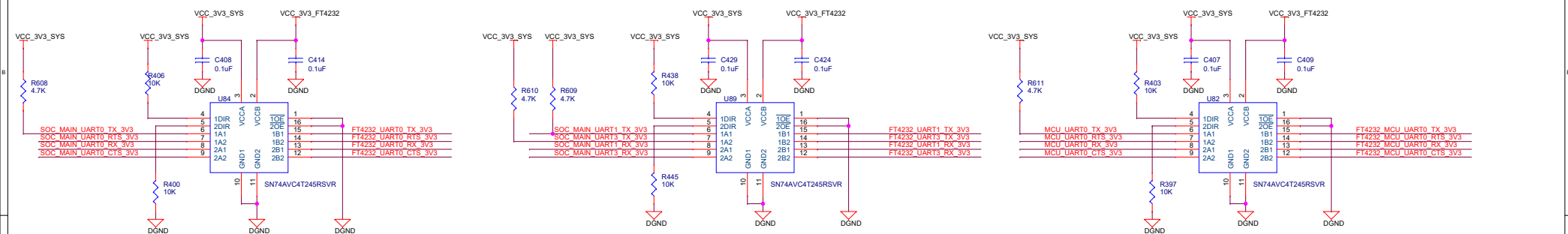
FT4232: 5V to 3.3V@500mA LDO



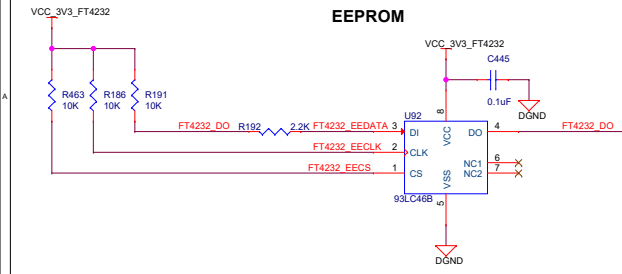
FT4232 UART



FT4232 LEVEL TRANSLATOR



EEPROM



Off Page Connections

SOC_MAIN_UART0_RX_3V3	SOC_MAIN_UART0_RX_3V3	29
SOC_MAIN_UART0_TX_3V3	SOC_MAIN_UART0_TX_3V3	29
SOC_MAIN_UART0_RTS_3V3	SOC_MAIN_UART0_RTS_3V3	29
SOC_MAIN_UART0_CTS_3V3	SOC_MAIN_UART0_CTS_3V3	29
MCU_UART0_RX_3V3	MCU_UART0_RX_3V3	34
MCU_UART0_TX_3V3	MCU_UART0_TX_3V3	34
MCU_UART0_RTS_3V3	MCU_UART0_RTS_3V3	34
MCU_UART0_CTS_3V3	MCU_UART0_CTS_3V3	34
SOC_MAIN_UART1_RX_3V3	SOC_MAIN_UART1_RX_3V3	29
SOC_MAIN_UART1_TX_3V3	SOC_MAIN_UART1_TX_3V3	29
SOC_MAIN_UART13_RX_3V3	SOC_MAIN_UART13_RX_3V3	29
SOC_MAIN_UART13_TX_3V3	SOC_MAIN_UART13_TX_3V3	29

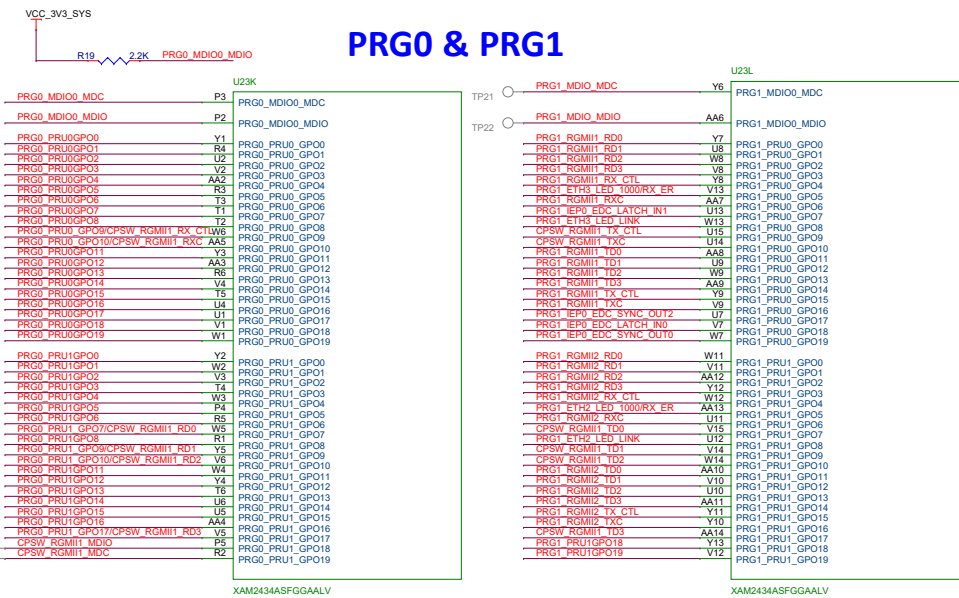
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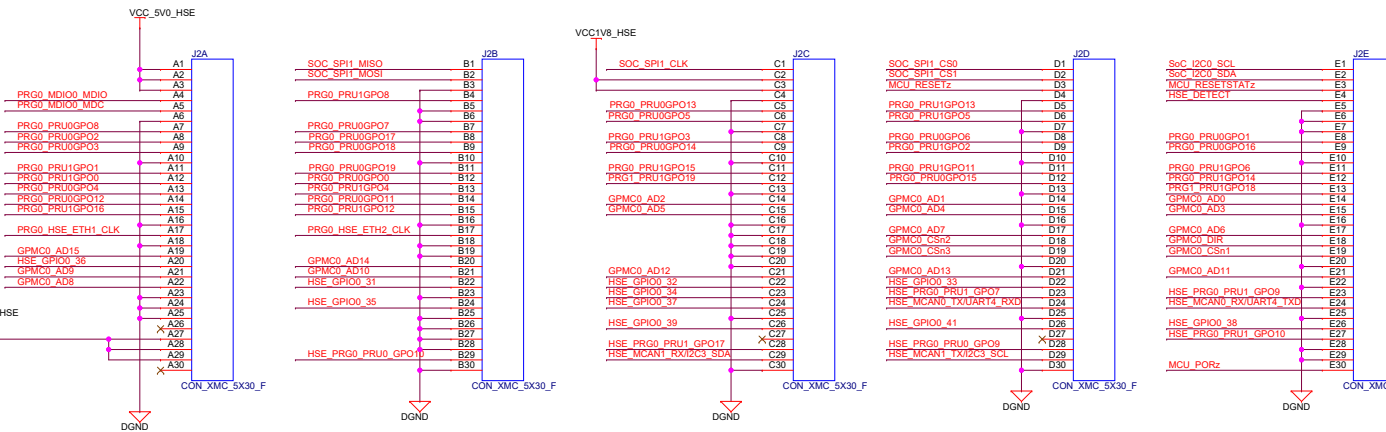
Title FT4232 UART to USB BRIDGE

Size	Variant Name = PROC101C(002) TMD5243GPEVM	Rev
C		E2
Date:	Monday, August 22, 2022	Sheet 26 of 40

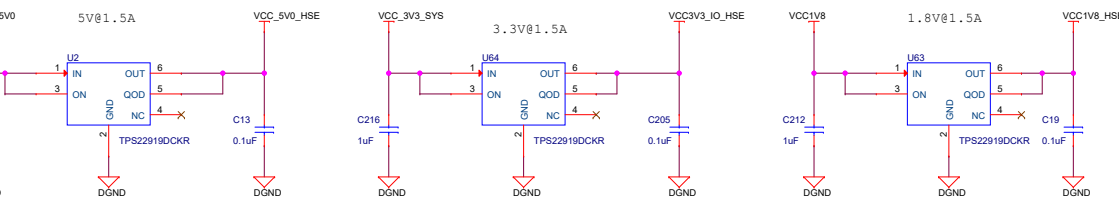
PRG0 & PRG1



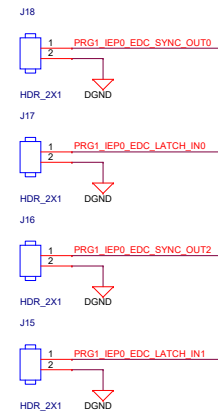
HIGH SPEED EXPANSION CONNECTOR



HSE CONNECTOR LOAD SWITCHES



SYNC TP



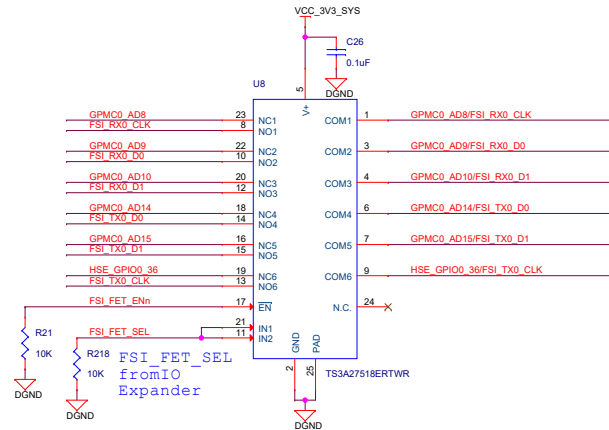
Off Page Connections

To Presence Detect Buffer	15	HSE_DETECT	<<<	HSE_DETECT1
From Processor GPMC	28	GPMC0_CSn1	<<<	GPMC0_CSn1
	28	GPMC0_CSn2	<<<	GPMC0_CSn2
	28	GPMC0_CSn3	<<<	GPMC0_CSn3
	28	GPMC0_DIR	<<<	GPMC0_DIR
From FSI mux	28	GPMC0_A08	<<<	GPMC0_A08
	28	GPMC0_A09	<<<	GPMC0_A09
	28	GPMC0_A10	<<<	GPMC0_A10
	28	GPMC0_A11	<<<	GPMC0_A11
	28	GPMC0_A15	<<<	GPMC0_A15
	28	HSE_GPI00_36	<<<	HSE_GPI00_36
From Processor GPMC resistor muxed with MIP1	28	GPMC0_A00	<<<	GPMC0_A00
	28	GPMC0_A01	<<<	GPMC0_A01
	28	GPMC0_A02	<<<	GPMC0_A02
	28	GPMC0_A03	<<<	GPMC0_A03
	28	GPMC0_A04	<<<	GPMC0_A04
	28	GPMC0_A05	<<<	GPMC0_A05
	28	GPMC0_A06	<<<	GPMC0_A06
	28	GPMC0_A07	<<<	GPMC0_A07
	28	GPMC0_A11	<<<	GPMC0_A11
	28	GPMC0_A12	<<<	GPMC0_A12
	28	GPMC0_A13	<<<	GPMC0_A13
	28	HSE_GPI00_30	<<<	HSE_GPI00_30
	28	HSE_GPI00_33	<<<	HSE_GPI00_33
	28	HSE_GPI00_34	<<<	HSE_GPI00_34
	28	HSE_GPI00_35	<<<	HSE_GPI00_35
	28	HSE_GPI00_36	<<<	HSE_GPI00_36
	28	HSE_GPI00_37	<<<	HSE_GPI00_37
	28	HSE_GPI00_38	<<<	HSE_GPI00_38
	28	HSE_GPI00_39	<<<	HSE_GPI00_39
	28	HSE_GPI00_40	<<<	HSE_GPI00_40
From Processor	34	MCU_PORz	<<<	MCU_PORz
	34,35	MCU_RESETz	<<<	MCU_RESETz
	34	MCU_RESESTATz	<<<	MCU_RESESTATz
	29	HSE_MCAN0_RXUART4_TX0	<<<	HSE_MCAN0_RXUART4_TX0
	29	HSE_MCAN0_TXUART4_RX0	<<<	HSE_MCAN0_TXUART4_RX0
	29	HSE_MCAN1_TXI2C3_SCL	<<<	HSE_MCAN1_TXI2C3_SCL
	29	HSE_MCAN1_TXI2C3_SCL	<<<	HSE_MCAN1_TXI2C3_SCL
	29	SOC_SP1_CLK	<<<	SOC_SP1_CLK
	29	SOC_SP1_M0S0	<<<	SOC_SP1_M0S0
	29	SOC_SP1_M0S1	<<<	SOC_SP1_M0S1
	29	SOC_SP1_MISO	<<<	SOC_SP1_MISO
	29	SOC_SP1_CS1	<<<	SOC_SP1_CS1
	15,29,33	Soc_I2C0_SCL	<<<	Soc_I2C0_SCL
	15,29,33	Soc_I2C0_SDA	<<<	Soc_I2C0_SDA
From clock Buffer	31	PRG0_HSE_ETH1_CLK	<<<	PRG0_HSE_ETH1_CLK
	31	PRG0_HSE_ETH2_CLK	<<<	PRG0_HSE_ETH2_CLK
To and from ICSSG1 RGMI1 2 Ethernet PHY	17	PRG1_RGMI1_R0	<<<	PRG1_RGMI1_R0
	17	PRG1_RGMI1_RD1	<<<	PRG1_RGMI1_RD1
	17	PRG1_RGMI1_R02	<<<	PRG1_RGMI1_R02
	17	PRG1_RGMI1_RXC	<<<	PRG1_RGMI1_RXC
	17	PRG1_RGMI1_RXC_CTL	<<<	PRG1_RGMI1_RXC_CTL
	17	PRG1_ETH2_LED_1000RX_ER	<<<	PRG1_ETH2_LED_1000RX_ER
	17	PRG1_RGMI1_T00	<<<	PRG1_RGMI1_T00
	17	PRG1_RGMI1_T01	<<<	PRG1_RGMI1_T01
	17	PRG1_ETH3_LED_LINK	<<<	PRG1_ETH3_LED_LINK
	17	PRG1_ETH2_LED_LINK	<<<	PRG1_ETH2_LED_LINK
	17	PRG1_RGMI1_R0	<<<	PRG1_RGMI1_R0
	17	PRG1_RGMI1_RD1	<<<	PRG1_RGMI1_RD1
	17	PRG1_RGMI1_R02	<<<	PRG1_RGMI1_R02
	17	PRG1_RGMI1_RXC	<<<	PRG1_RGMI1_RXC
	17	PRG1_RGMI1_RXC_CTL	<<<	PRG1_RGMI1_RXC_CTL
	17,18	PRG1_ETH3_LED_1000RX_ER	<<<	PRG1_ETH3_LED_1000RX_ER
	17,18	PRG1_ETH3_LED_LINK	<<<	PRG1_ETH3_LED_LINK
	17,18	PRG1_ETH2_LED_LINK	<<<	PRG1_ETH2_LED_LINK
	18	PRG1_RGMI1_R0	<<<	PRG1_RGMI1_R0
	18	PRG1_RGMI1_RD1	<<<	PRG1_RGMI1_RD1
	18	PRG1_RGMI1_R02	<<<	PRG1_RGMI1_R02
	18	PRG1_RGMI1_RXC	<<<	PRG1_RGMI1_RXC
	18	PRG1_RGMI1_RXC_CTL	<<<	PRG1_RGMI1_RXC_CTL
	18	PRG1_ETH3_LED_1000RX_ER	<<<	PRG1_ETH3_LED_1000RX_ER
	18	PRG1_RGMI1_T00	<<<	PRG1_RGMI1_T00
	18	PRG1_RGMI1_T01	<<<	PRG1_RGMI1_T01
	18	PRG1_RGMI1_T02	<<<	PRG1_RGMI1_T02
	18	PRG1_RGMI1_T03	<<<	PRG1_RGMI1_T03
	18	PRG1_RGMI1_TXC	<<<	PRG1_RGMI1_TXC
	18	PRG1_RGMI1_TXC_CTL	<<<	PRG1_RGMI1_TXC_CTL
From MUX To HSE	16	HSE_PRG0_PRUI1_GPO7	<<<	HSE_PRG0_PRUI1_GPO7
	16	HSE_PRG0_PRUI1_GPO9	<<<	HSE_PRG0_PRUI1_GPO9
	16	HSE_PRG0_PRUI1_GPO10	<<<	HSE_PRG0_PRUI1_GPO10
	16	HSE_PRG0_PRUI1_GPO11	<<<	HSE_PRG0_PRUI1_GPO11
	16	HSE_PRG0_PRUI1_GPO12	<<<	HSE_PRG0_PRUI1_GPO12
	16	HSE_PRG0_PRUI1_GPO13	<<<	HSE_PRG0_PRUI1_GPO13
	16	HSE_PRG0_PRUI1_GPO14	<<<	HSE_PRG0_PRUI1_GPO14
	16	HSE_PRG0_PRUI1_GPO15	<<<	HSE_PRG0_PRUI1_GPO15
	16	HSE_PRG0_PRUI1_GPO16	<<<	HSE_PRG0_PRUI1_GPO16
	16	HSE_PRG0_PRUI1_GPO17	<<<	HSE_PRG0_PRUI1_GPO17
	16	HSE_PRG0_PRUI1_GPO18	<<<	HSE_PRG0_PRUI1_GPO18
	16	HSE_PRG0_PRUI1_GPO19	<<<	HSE_PRG0_PRUI1_GPO19
	16	HSE_PRG0_PRUI1_GPO20	<<<	HSE_PRG0_PRUI1_GPO20
	16	HSE_PRG0_PRUI1_GPO21	<<<	HSE_PRG0_PRUI1_GPO21
	16	HSE_PRG0_PRUI1_GPO22	<<<	HSE_PRG0_PRUI1_GPO22
	16	HSE_PRG0_PRUI1_GPO23	<<<	HSE_PRG0_PRUI1_GPO23
	16	HSE_PRG0_PRUI1_GPO24	<<<	HSE_PRG0_PRUI1_GPO24
	16	HSE_PRG0_PRUI1_GPO25	<<<	HSE_PRG0_PRUI1_GPO25
	16	HSE_PRG0_PRUI1_GPO26	<<<	HSE_PRG0_PRUI1_GPO26
	16	HSE_PRG0_PRUI1_GPO27	<<<	HSE_PRG0_PRUI1_GPO27
	16	HSE_PRG0_PRUI1_GPO28	<<<	HSE_PRG0_PRUI1_GPO28
	16	HSE_PRG0_PRUI1_GPO29	<<<	HSE_PRG0_PRUI1_GPO29
	16	HSE_PRG0_PRUI1_GPO30	<<<	HSE_PRG0_PRUI1_GPO30
	16	HSE_PRG0_PRUI1_GPO31	<<<	HSE_PRG0_PRUI1_GPO31
	16	HSE_PRG0_PRUI1_GPO32	<<<	HSE_PRG0_PRUI1_GPO32
	16	HSE_PRG0_PRUI1_GPO33	<<<	HSE_PRG0_PRUI1_GPO33
	16	HSE_PRG0_PRUI1_GPO34	<<<	HSE_PRG0_PRUI1_GPO34
	16	HSE_PRG0_PRUI1_GPO35	<<<	HSE_PRG0_PRUI1_GPO35
	16	HSE_PRG0_PRUI1_GPO36	<<<	HSE_PRG0_PRUI1_GPO36
	16	HSE_PRG0_PRUI1_GPO37	<<<	HSE_PRG0_PRUI1_GPO37
	16	HSE_PRG0_PRUI1_GPO38	<<<	HSE_PRG0_PRUI1_GPO38
	16	HSE_PRG0_PRUI1_GPO39	<<<	HSE_PRG0_PRUI1_GPO39
	16	HSE_PRG0_PRUI1_GPO40	<<<	HSE_PRG0_PRUI1_GPO40
	16	HSE_PRG0_PRUI1_GPO41	<<<	HSE_PRG0_PRUI1_GPO41
	16	HSE_PRG0_PRUI1_GPO42	<<<	HSE_PRG0_PRUI1_GPO42
	16	HSE_PRG0_PRUI1_GPO43	<<<	HSE_PRG0_PRUI1_GPO43
	16	HSE_PRG0_PRUI1_GPO44	<<<	HSE_PRG0_PRUI1_GPO44
	16	HSE_PRG0_PRUI1_GPO45	<<<	HSE_PRG0_PRUI1_GPO45
	16	HSE_PRG0_PRUI1_GPO46	<<<	HSE_PRG0_PRUI1_GPO46
	16	HSE_PRG0_PRUI1_GPO47	<<<	HSE_PRG0_PRUI1_GPO47
	16	HSE_PRG0_PRUI1_GPO48	<<<	HSE_PRG0_PRUI1_GPO48
	16	HSE_PRG0_PRUI1_GPO49	<<<	HSE_PRG0_PRUI1_GPO49
	16	HSE_PRG0_PRUI1_GPO50	<<<	HSE_PRG0_PRUI1_GPO50
	16	HSE_PRG0_PRUI1_GPO51	<<<	HSE_PRG0_PRUI1_GPO51
	16	HSE_PRG0_PRUI1_GPO52	<<<	HSE_PRG0_PRUI1_GPO52
	16	HSE_PRG0_PRUI1_GPO53	<<<	HSE_PRG0_PRUI1_GPO53
	16	HSE_PRG0_PRUI1_GPO54	<<<	HSE_PRG0_PRUI1_GPO54
	16	HSE_PRG0_PRUI1_GPO55	<<<	HSE_PRG0_PRUI1_GPO55
	16	HSE_PRG0_PRUI1_GPO56	<<<	HSE_PRG0_PRUI1_GPO56
	16	HSE_PRG0_PRUI1_GPO57	<<<	HSE_PRG0_PRUI1_GPO57
	16	HSE_PRG0_PRUI1_GPO58	<<<	HSE_PRG0_PRUI1_GPO58
	16	HSE_PRG0_PRUI1_GPO59	<<<	HSE_PRG0_PRUI1_GPO59
	16	HSE_PRG0_PRUI1_GPO60	<<<	HSE_PRG0_PRUI1_GPO60
	16	HSE_PRG0_PRUI1_GPO61	<<<	HSE_PRG0_PRUI1_GPO61
	16	HSE_PRG0_PRUI1_GPO62	<<<	HSE_PRG0_PRUI1_GPO62
	16	HSE_PRG0_PRUI1_GPO63	<<<	HSE_PRG0_PRUI1_GPO63
	16	HSE_PRG0_PRUI1_GPO64	<<<	HSE_PRG0_PRUI1_GPO64
	16	HSE_PRG0_PRUI1_GPO65	<<<	HSE_PRG0_PRUI1_GPO65
	16	HSE_PRG0_PRUI1_GPO66	<<<	HSE_PRG0_PRUI1_GPO66
	16	HSE_PRG0_PRUI1_GPO67	<<<	HSE_PRG0_PRUI1_GPO67
	16	HSE_PRG0_PRUI1_GPO68	<<<	HSE_PRG0_PRUI1_GPO68
	16	HSE_PRG0_PRUI1_GPO69	<<<	HSE_PRG0_PRUI1_GPO69
	16	HSE_PRG0_PRUI1_GPO70	<<<	HSE_PRG0_PRUI1_GPO70
	16	HSE_PRG0_PRUI1_GPO71	<<<	HSE_PRG0_PRUI1_GPO71
	16	HSE_PRG0_PRUI1_GPO72	<<<	HSE_PRG0_PRUI1_GPO72
	16	HSE_PRG0_PRUI1_GPO73	<<<	HSE_PRG0_PRUI1_GPO73
	16	HSE_PRG0_PRUI1_GPO74	<<<	HSE_PRG0_PRUI1_GPO74
	16	HSE_PRG0_PRUI1_GPO75	<<<	HSE_PRG0_PRUI1_GPO75
	16	HSE_PRG0_PRUI1_GPO76	<<<	HSE_PRG0_PRUI1_GPO76
	16	HSE_PRG0_PRUI1_GPO77	<<<	HSE_PRG0_PRUI1_GPO77
	16	HSE_PRG0_PRUI1_GPO78	<<<	HSE_PRG0_PRUI1_GPO78
	16	HSE_PRG0_PRUI1_GPO79	<<<	HSE_PRG0_PRUI1_GPO79
	16	HSE_PRG0_PRUI1_GPO80	<<<	HSE_PRG0_PRUI1_GPO80
	16	HSE_PRG0_PRUI1_GPO81	<<<	HSE_PRG0_PRUI1_GPO81
	16	HSE_PRG0_PRUI1_GPO82	<<<	HSE_PRG0_PRUI1_GPO82
	16	HSE_PRG0_PRUI1_GPO83	<<<	HSE_PRG0_PRUI1_GPO83
	16	HSE_PRG0_PRUI1_GPO84	<<<	HSE_PRG0_PRUI1_GPO84
	16	HSE_PRG0_PRUI1_GPO85	<<<	HSE_PRG0_PRUI1_GPO85
	16	HSE_PRG0_PRUI1_GPO86	<<<	HSE_PRG0_PRUI1_GPO86
	16	HSE_PRG0_PRUI1_GPO87	<<<	HSE_PRG0_PRUI1_GPO87
	16	HSE_PRG0_PRUI1_GPO88	<<<	HSE_PRG0_PRUI1_GPO88
	16	HSE_PRG0_PRUI1_GPO89	<<<	HSE_PRG0_PRUI1_GPO89
	16	HSE_PRG0_PRUI1_GPO90	<<<	HSE_PRG0_PRUI1_GPO90
	16	HSE_PRG0_PRUI1_GPO91	<<<	HSE_PRG0_PRUI1_GPO91
	16	HSE_PRG0_PRUI1_GPO92	<<<	HSE_PRG0_PRUI1_GPO92
	16	HSE_PRG0_PRUI1_GPO93	<<<	HSE_PRG0_PRUI1_GPO93
	16	HSE_PRG0_PRUI1_GPO94	<<<	HSE_PRG0_PRUI1_GPO94
	16	HSE_PRG0_PRUI1_GPO95	<<<	HSE_PRG0_PRUI1_GPO95
	16	HSE_PRG0_PRUI1_GPO96	<<<	HSE_PRG0_PRUI1_GPO96
	16	HSE_PRG0_PRUI1_GPO97	<<<	HSE_PRG0_PRUI1_GPO97
	16	HSE_PRG0_PRUI1_GPO98	<<<	HSE_PRG0_PRUI1_GPO98
	16	HSE_PRG0_PRUI1_GPO99	<<<	HSE_PRG0_PRUI1_GPO99
	16	HSE_PRG0_PRUI1_GPO100	<<<	HSE_PRG0_PRUI1_GPO100
	16	HSE_PRG0_PRUI1_GPO101	<<<	HSE_PRG0_PRUI1_GPO101
	16	HSE_PRG0_PRUI1_GPO102	<<<	HSE_PRG0_PRUI1_GPO102
	16	HSE_PRG0_PRUI1_GPO103	<<<	HSE_PRG0_PRUI1_GPO103
	16	HSE_PRG0_PRUI1_GPO104	<<<	HSE_PRG0_PRUI1_GPO104
	16	HSE_PRG0_PRUI1_GPO105	<<<	HSE_PRG0_PRUI1_GPO105
	16	HSE_PRG0_PRUI1_GPO106	<<<	HSE_PRG0_PRUI1_GPO106
	16	HSE_PRG0_PRUI1_GPO107	<<<	HSE_PRG0_PRUI1_GPO107
	16	HSE_PRG0_PRUI1_GPO108	<<<	HSE_PRG0_PRUI1_GPO108
	16	HSE_PRG0_PRUI1_GPO109	<<<	HSE_PRG0_PRUI1_GPO109
	16	HSE_PRG0_PRUI1_GPO110	<<<	HSE_PRG0_PRUI1_GPO110
	16	HSE_PRG0_PRUI1_GPO111	<<<	HSE_PRG0_PRUI1_GPO111
	16	HSE_PRG0_PRUI1_GPO112	<<<	HSE_PRG0_PRUI1_GPO112
	16	HSE_PRG0_PRUI1_GPO113	<<<	HSE_PRG0_PRUI1_GPO113
	16	HSE_PRG0_PRUI1_GPO114	<<<	HSE_PRG0_PRUI1_GPO114
	16	HSE_PRG0_PRUI1_GPO115	<<<	HSE_PRG0_PRUI1_GPO115
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	16	HSE_PRG0_PRUI1_GPO117	<<<	HSE_PRG0_PRUI1_GPO117
	16	HSE_PRG0_PRUI1_GPO118	<<<	HSE_PRG0_PRUI1_GPO118
	16	HSE_PRG0_PRUI1_GPO119	<<<	HSE_PRG0_PRUI1_GPO119
	16	HSE_PRG0_PRUI1_GPO120	<<<	HSE_PRG0_PRUI1_GPO120
	16	HSE_PRG0_PRUI1_GPO121	<<<	HSE_PRG0_PRUI1_GPO121
	16	HSE_PRG0_PRUI1_GPO122	<<<	HSE_PRG0_PRUI1_GPO122
	16	HSE_PRG0_PRUI1_GPO123	<<<	HSE_PRG0_PRUI1_GPO123
	16	HSE_PRG0_PRUI1_GPO124	<<<	HSE_PRG0_PRUI1_GPO124
	16	HSE_PRG0_PRUI1_GPO125	<<<	HSE_PRG0_PRUI1_GPO125
	16	HSE_PRG0_PRUI1_GPO126	<<<	HSE_PRG0_PRUI1_GPO126
	16	HSE_PRG0_PRUI1_GPO127	<<<	HSE_PRG0_PRUI1_GPO127
	16	HSE_PRG0_PRUI1_GPO128	<<<	HSE_PRG0_PRUI1_GPO128
	16	HSE_PRG0_PRUI1_GPO129	<<<	HSE_PRG0_PRUI1_GPO129
	16	HSE_PRG0_PRUI1_GPO130	<<<	HSE_PRG0_PRUI1_GPO130
	16	HSE_PRG0_PRUI1_GPO131	<<<	HSE_PRG0_PRUI1_GPO131
	16	HSE_PRG0_PRUI1_GPO132	<<<	HSE_PRG0_PRUI1_GPO132
	16	HSE_PRG0_PRUI1_GPO133	<<<	HSE_PRG0_PRUI1_GPO133
	16	HSE_PRG0_PRUI1_GPO134	<<<	HSE_PRG0_PRUI1_GPO134
	16	HSE_PRG0_PRUI1_GPO135	<<<	HSE_PRG0_PRUI1_GPO135
	16	HSE_PRG0_PRUI1_GPO136	<<<	HSE_PRG0_PRUI1_GPO136
	16	HSE_PRG0_PRUI1_GPO137	<<<	HSE_PRG0_PRUI1_GPO137
	16	HSE_PRG0_PRUI1_GPO138	<<<	HSE_PRG0_PRUI1_GPO138
	16	HSE_PRG0_PRUI1_GPO139	<<<	HSE_PRG0_PRUI1_GPO139
	16	HSE_PRG0_PRUI1_GPO140	<<<	HSE_PRG0_PRUI1_GPO140
	16	HSE_PRG0_PRUI1_GPO141	<<<	HSE_PRG0_PRUI1_GPO141
	16	HSE_PRG0_PRUI1_GPO142	<<<	HSE_PRG0_PRUI1_GPO142
	16	HSE_PRG0_PRUI1_GPO143	<<<	HSE_PRG0_PRUI1_GPO143
	16	HSE_PRG0_PRUI1_GPO144	<<<	HSE_PRG0_PRUI1_GPO144
	16	HSE_PRG0_PRUI1_GPO145	<<<	HSE_PRG0_PRUI1_GPO145
	16	HSE_PRG0_PRUI1_GPO146	<<<	HSE_PRG0_PRUI1_GPO146
	16	HSE_PRG0_PRUI1_GPO147	<<<	HSE_PRG0_PRUI1_GPO147
	16	HSE_PRG0_PRUI1_GPO148	<<<	HSE_PRG0_PRUI1_GPO148
	16	HSE_PRG0_PRUI1_GPO149	<<<	HSE_PRG0_PRUI1_GPO149
	16	HSE_PRG0_PRUI1_GPO150	<<<	HSE_PRG0_PRUI1_GPO150
	16	HSE_PRG0_PRUI1_GPO151	<<<	HSE_PRG0_PRUI1_GPO151
	16	HSE_PRG0_PRUI1_GPO152	<<<	HSE_PRG0_PRUI1_GPO152
	16	HSE_PRG0_PRUI1_GPO153	<<<	HSE_PRG0_PRUI1_GPO153
	16	HSE_PRG0_PRUI1_GPO154	<<<	HSE_PRG0_PRUI1_GPO154

GPMC



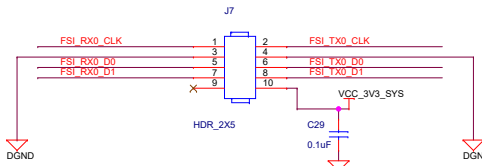
GPMC TO FSI & HSE CONNECTOR



TS3A2751BRTWR Truth Table

EN#	IN1	IN2	NC1/2/3 TO COM1/2/3 & COM1/2/3 TO NC1/2/3	NC4/5/6 TO COM1/2/3 & COM1/2/3 TO NC4/5/6	NO1/2/3 TO COM1/2/3 & COM1/2/3 TO NO1/2/3	NO4/5/6 TO COM1/2/3 & COM1/2/3 TO NO4/5/6
H	X	X	OFF	OFF	OFF	OFF
L	L	L	ON	ON	OFF	OFF
L	H	L	OFF	ON	ON	OFF
L	L	H	ON	OFF	OFF	ON
L	H	H	OFF	OFF	ON	ON

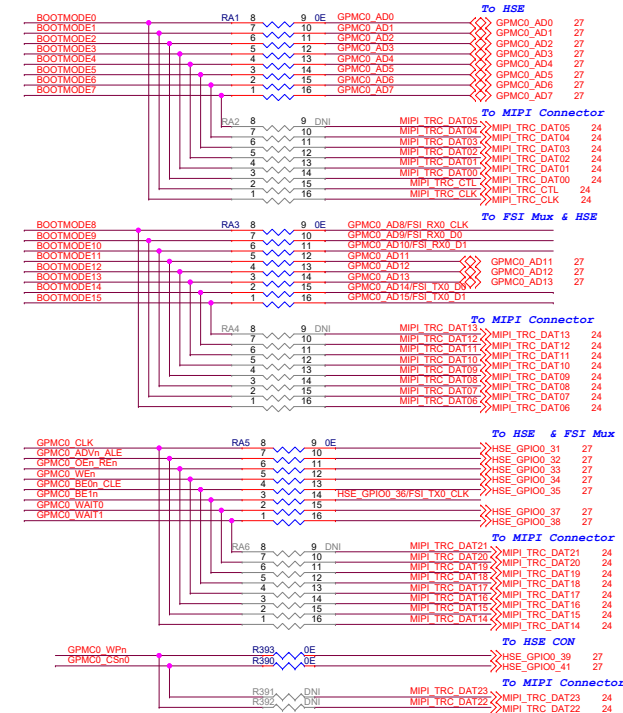
FSI CONNECTOR



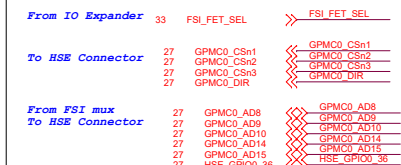
0- Ohm Res MUX between HSE Connector and TRACE Functionality

-For HSE Connector RA1, RA3, RA5, R393 & R390 Should be installed and RA2, RA4, RA6, R391 & R392 Should be DNI'd.

-For TRACE RA2, RA4, RA6, R391 & R392 Should be installed and RA1, RA3, RA5, R393 & R390 Should be DNI'd.



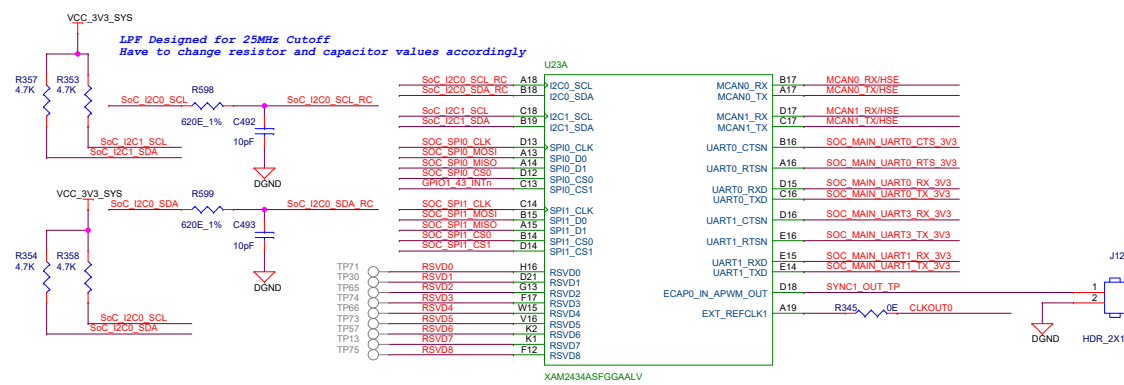
Off Page Connections



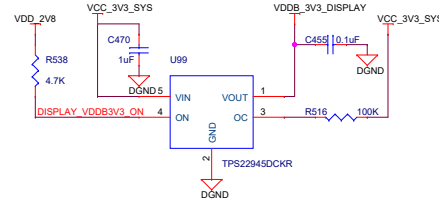
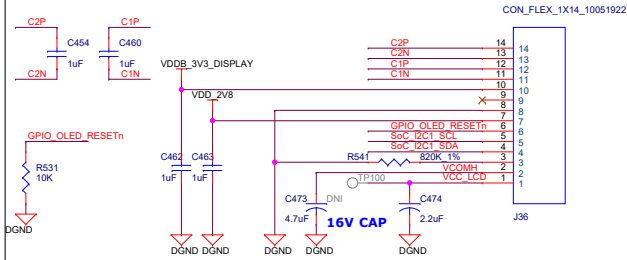
Designed for TI by Mistral Solutions Pvt Ltd



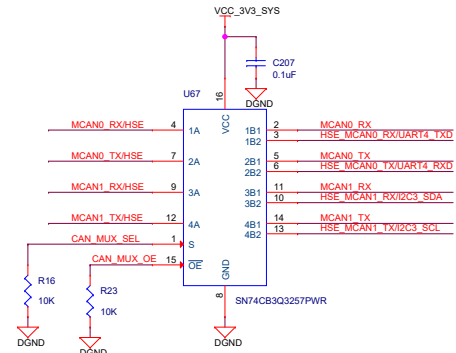
Title		GPMC	
Size	Variant Name = PROC101C(002) TMD2S243GPEVM	Rev	
C		E2	
Date:	Monday, August 22, 2022	Sheet	28 of 40



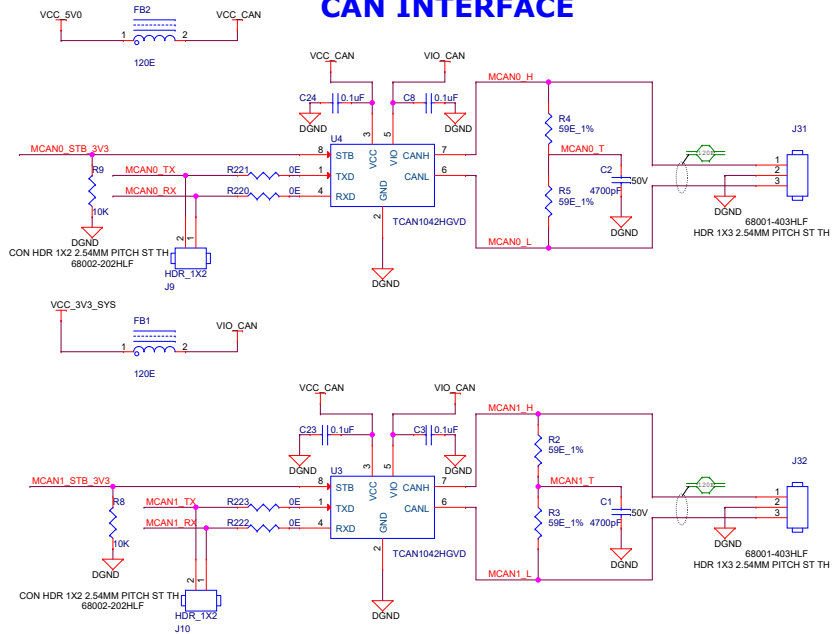
DISPLAY CONNECTOR



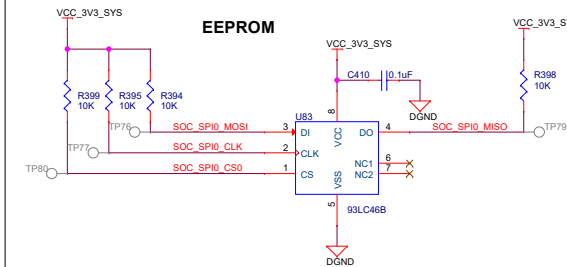
HSE/CAN MUX



CAN INTERFACE



SPI EEPROM



Off Page Connections

From Debounce Circuit	GPIO1_43_INTn	35
From IO Expander	GPIO_OLED_RESETn	33
From IO Expander	MCAN1_STB_3V3	33
From IO Expander	MCAN0_STB_3V3	33
From IO Expander	CAN_MUX_SEL	33
From HSE Connector	HSE_MCAN0_RX/UART4_TXD	27
From HSE Connector	HSE_MCAN0_TX/UART4_RXD	27
From HSE Connector	HSE_MCAN1_RX/UART3_SDA	27
From HSE Connector	HSE_MCAN1_TX/UART3_SCL	27
From HSE Connector	SOC_SPI0_CLK	27
From HSE Connector	SOC_SPI0_MISO	27
From HSE Connector	SOC_SPI0_MOSI	27
From HSE Connector	SOC_SPI0_CS0	27
From HSE Connector	SOC_SPI0_CS1	27
From HSE Connector	SOC_I2C0_SCL	15,27,33
From HSE Connector	SOC_I2C0_SDA	15,27,33
From HSE Connector	SOC_I2C1_SCL	15,19,21,30,31,32,33
From HSE Connector	SOC_I2C1_SDA	15,19,21,30,31,32,33
From HSE Connector	CLKOUT0	31
From Clock Buffer	SOC_MAIN_UART0_TX_3V3	26
From Clock Buffer	SOC_MAIN_UART0_RX_3V3	26
From Clock Buffer	SOC_MAIN_UART0_CTS_3V3	26
From Clock Buffer	SOC_MAIN_UART0_RTS_3V3	26
From FT4232 Bridge	SOC_MAIN_UART1_TX_3V3	26
From FT4232 Bridge	SOC_MAIN_UART1_RX_3V3	26
From FT4232 Bridge	SOC_MAIN_UART1_CTS_3V3	26
From FT4232 Bridge	SOC_MAIN_UART1_RTS_3V3	26

PROC101C(02) TMS2433PEVM

Project :

Designed for TI by Mistral Solutions Pvt Ltd

<Project Name>



Title

CAN & DISPLAY INTERFACE

Size

Document Number

C

MS_TI_MAXIE_APPLICATION_CARD_SCH_REVA

Date:

Monday, August 22, 2022

Sheet

29

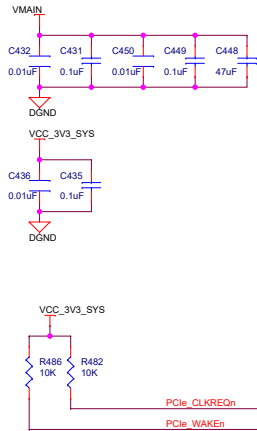
of

40

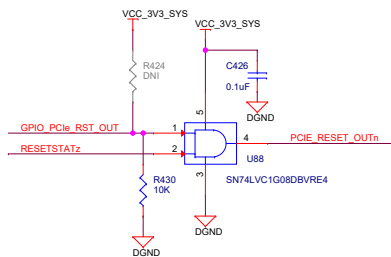
Rev

E2

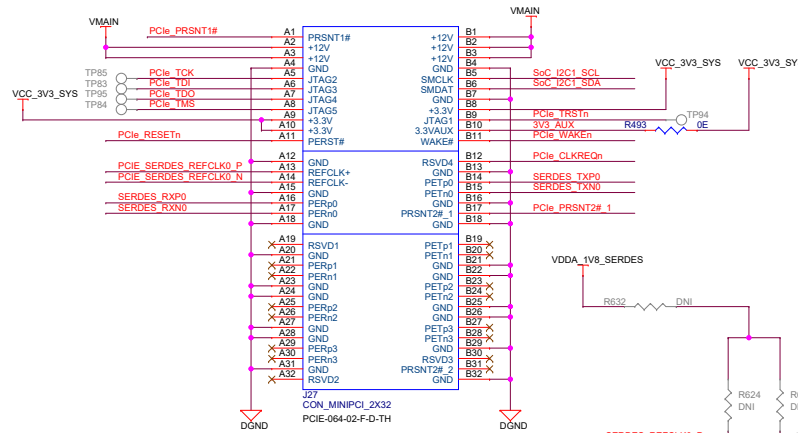
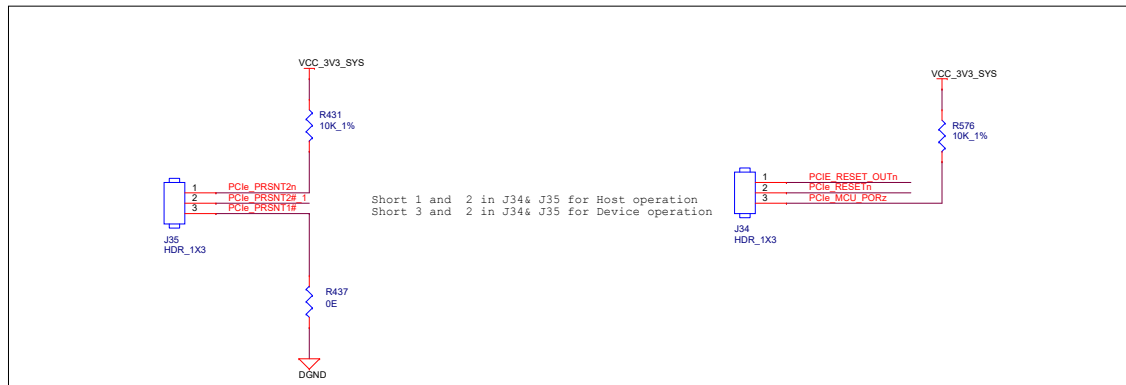
x4 Lane PCIe Connector



PCIe Reset

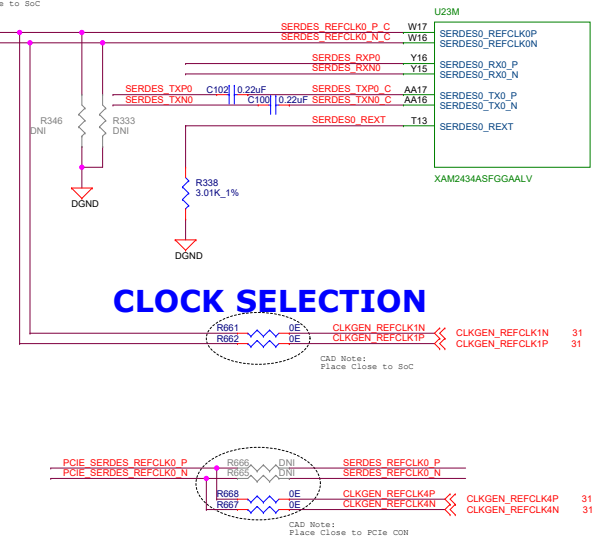


RC OR EP MODE SELECTION



Note:
R679 , R680 Mounted with 0E Resistor when PCIe REFCLK is in no Re-biasing Mode.
R679 , R680 to be replaced with 100nf CAP 0402 package when PCIe REFCLK is in Re-biasing Mode.

CLOCK SELECTION



Off Page Connections

PCIE MCU PORz	PCIE_MCU_PORz	34
GPIO_Pcie_RST_OUT	GPIO_Pcie_RST_OUT	33
RESESTATz	RESESTATz	13,14,20,31,33,34
SoC_I2C1_SCL	SoC_I2C1_SCL	15,19,21,29,31,32,33
SoC_I2C1_SDA	SoC_I2C1_SDA	15,19,21,29,31,32,33

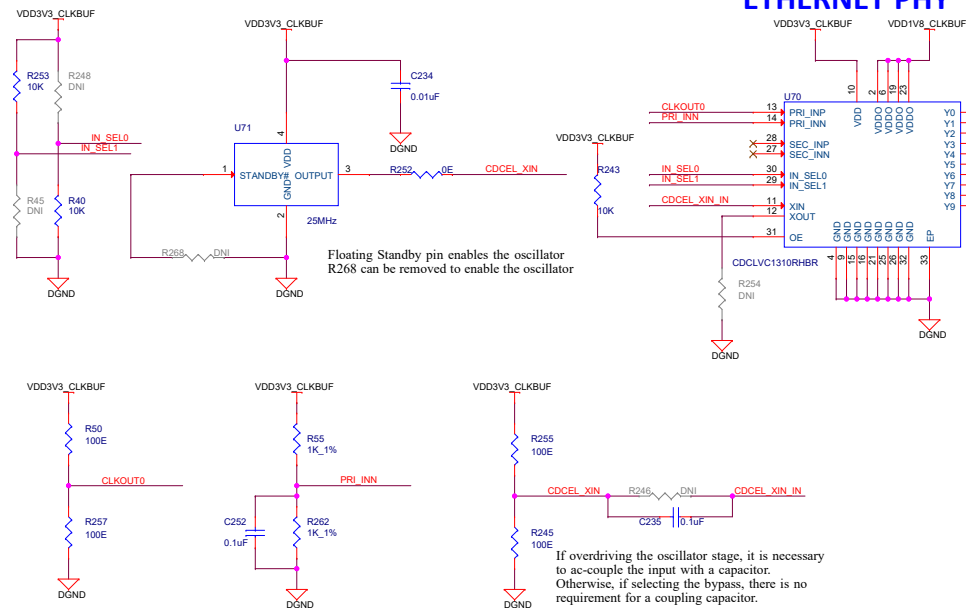
Designed for TI by Mistral Solutions Pvt Ltd



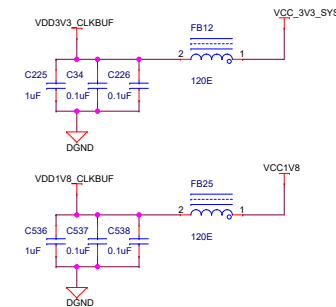
Title		
PCIe INTERFACE		
Size	PROC101C(002) TMS243GPEVM	Rev
C		E2
Date:	Monday, August 22, 2022	Sheet 30 of 40

REFERENCE INPUT SELECTION

ETHERNET PHY CLOCK BUFFER



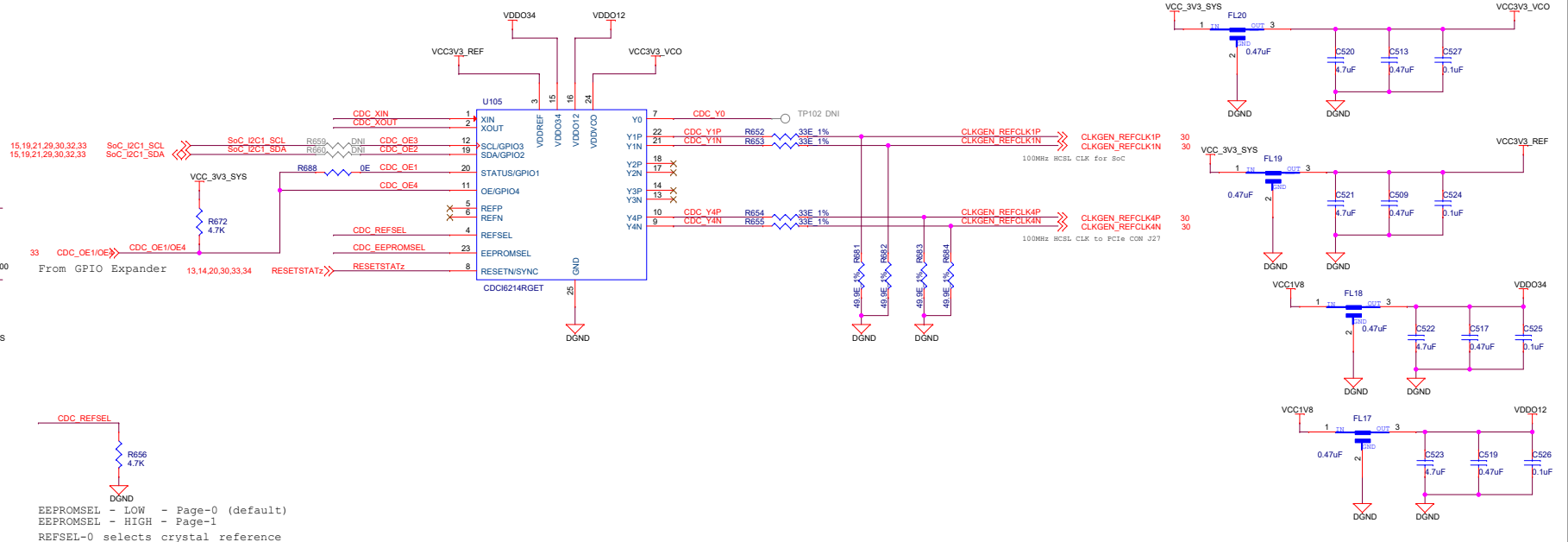
PROVIDING 2 CLOCK FOR HSE



Off Page Connections

From SoC CLKOUT0 << CLKOUT0 29

PCIe Clock HCSL (100MHz)



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Title ETHERNET PHY & PCIe CLOCK GENERATOR

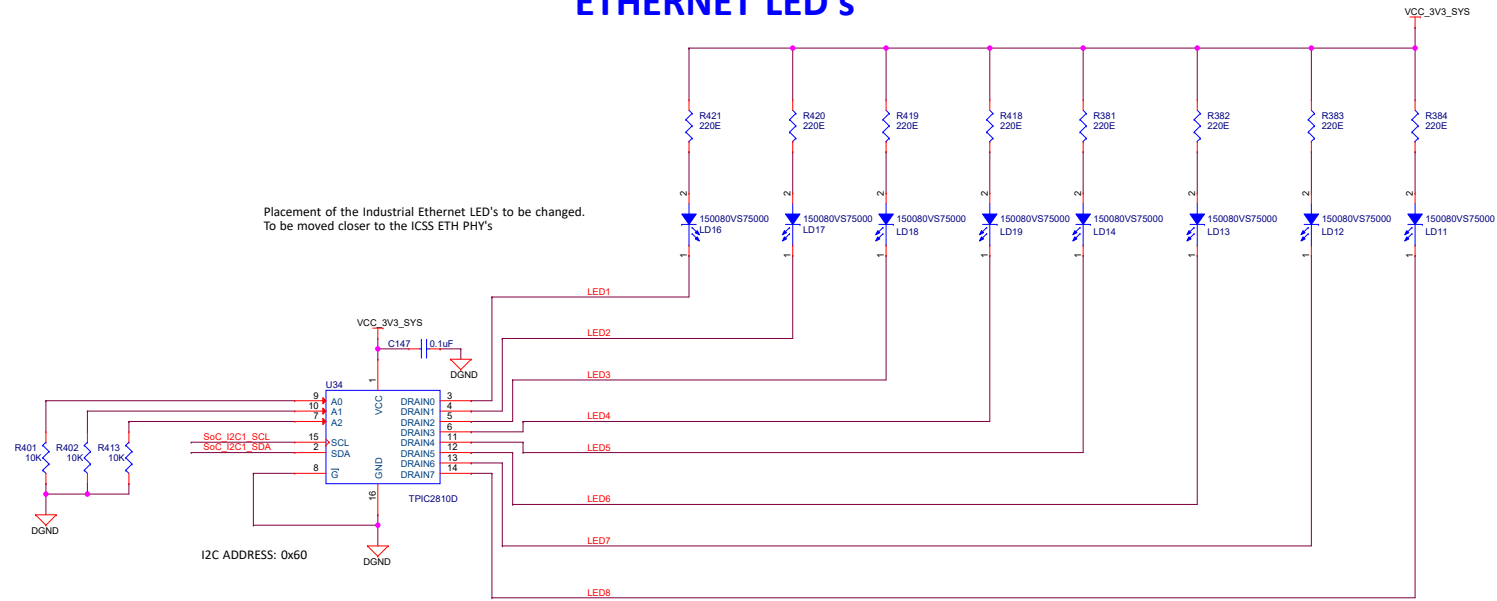
Size Variant Name = PROC101C(002) TMD8243GPEVM

Date: Monday, August 22, 2022

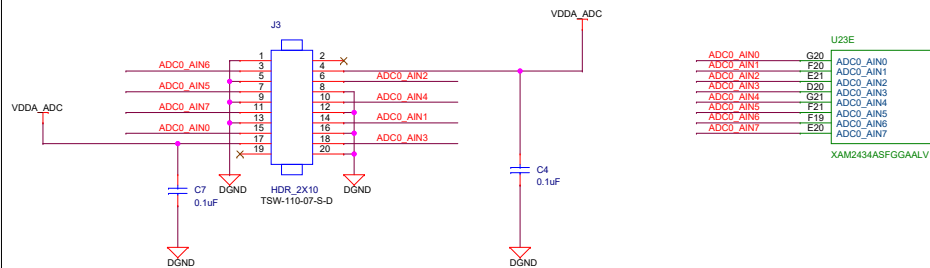
Rev E2

Sheet 31 of 40

ETHERNET LED's



ADC CONNECTOR



Off Page Connections

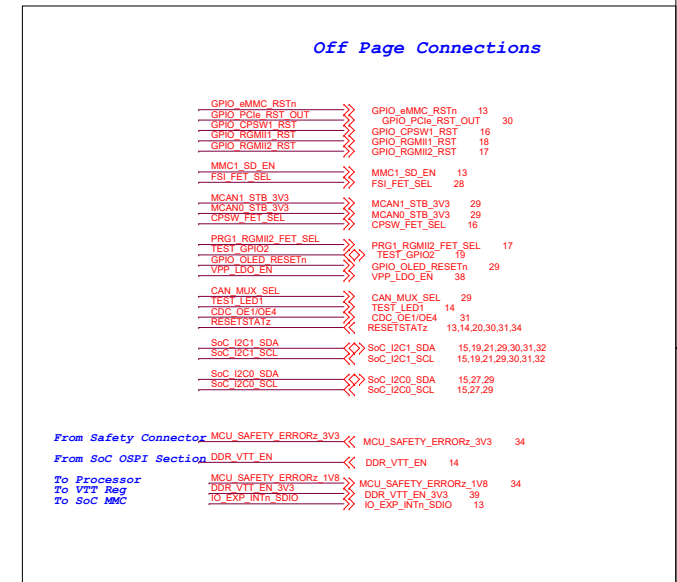
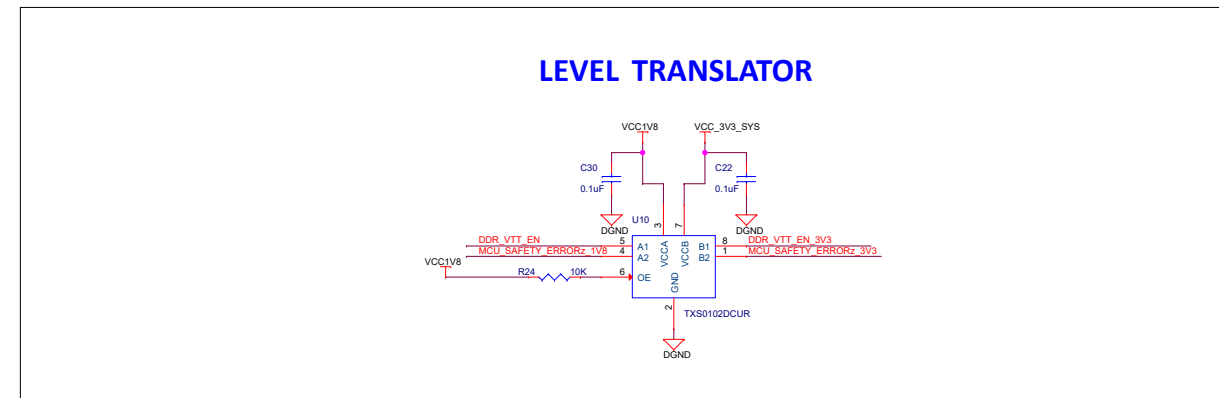
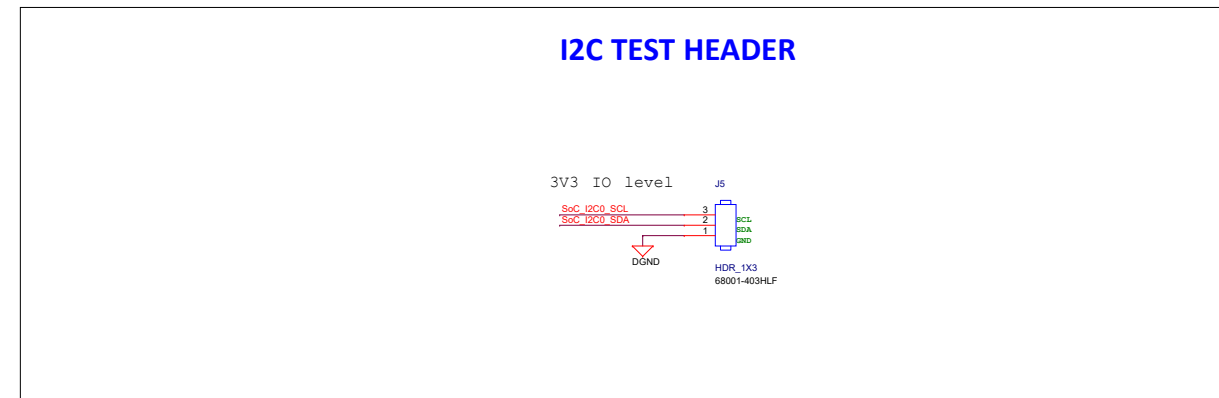
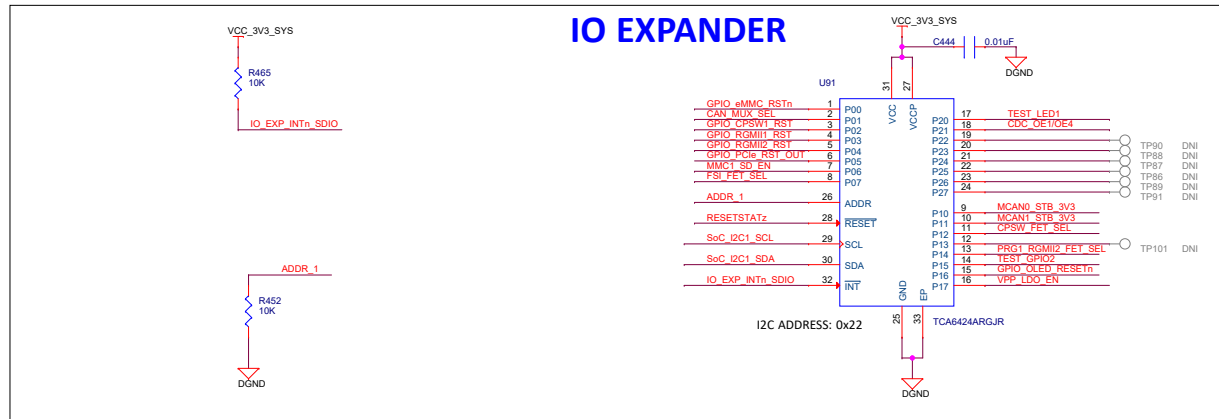
SoC_I2C1_SCL	SoC_I2C1_SCL	15,19,21,29,30,31,33
SoC_I2C1_SDA	SoC_I2C1_SDA	15,19,21,29,30,31,33

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Title ETHERNET LED's

Size	Variant Name = PROC101C(002) TMD5243GPEVM	Rev
C		E2
Date:	Monday, August 22, 2022	Sheet 32 of 40

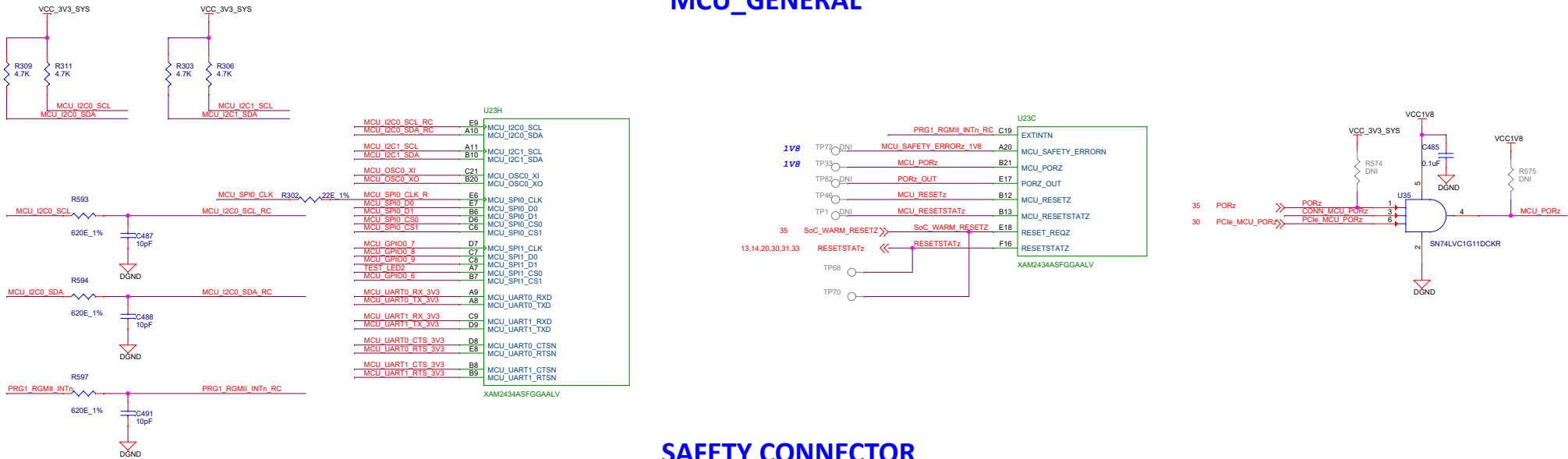


Designed for TI by Mistral Solutions Pvt Ltd



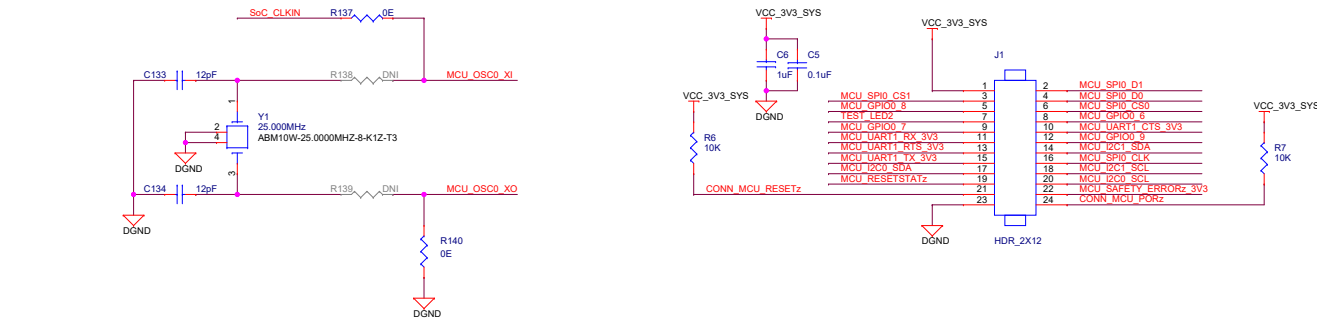
Title IO EXPANDER		
Size	Variant Name = PROC101C(002) TMD5243GPEVM	Rev E2
Date: Monday, August 22, 2022	Sheet 33 of 40	

MCU_GENERAL

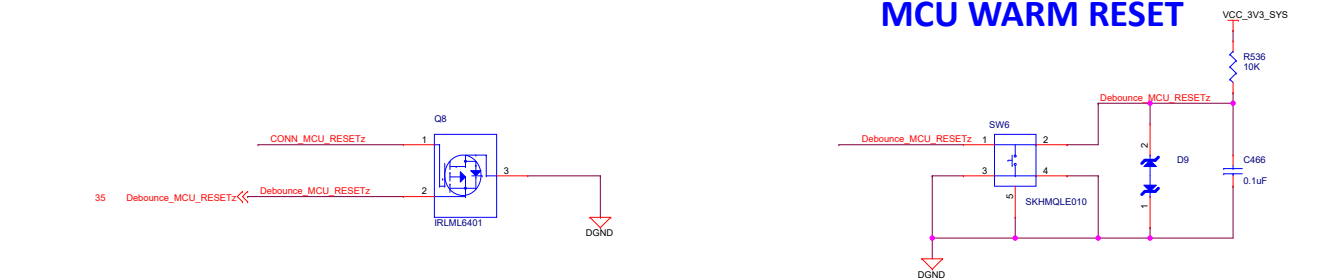


SAFETY CONNECTOR

LPF Designed for 25MHz Cutoff
Have to change resistor and capacitor values accordingly



MCU WARM RESET



Off Page Connections

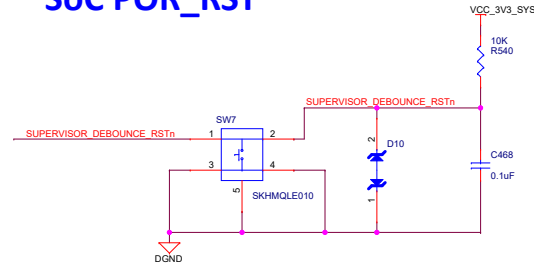
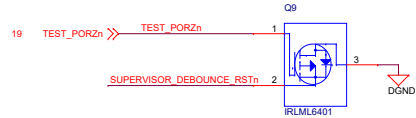
To HSE Connector	MCU_PORz	MCU_PORz	27
To Level translator	MCU_RESETz	MCU_RESETz	27,35
From Level translator	MCU_RESETSTATz	MCU_RESETSTATz	27
To Boot Mode Section	MCU_SAFETY_ERRORz_3V3	MCU_SAFETY_ERRORz_3V3	33
	MCU_SAFETY_ERRORz_1V8	MCU_SAFETY_ERRORz_1V8	33
	PORz_OUT	PORz_OUT	13,16,17,18,20
From ICSSG Phy142	PRG1_RGMII_INTn	PRG1_RGMII_INTn	16,17,18
To User LED	TEST_LED2	TEST_LED2	14
From Push button Switch	MCU_GPIO0_6	MCU_GPIO0_6	35
	SoC_CLKIN	SoC_CLKIN	31
	MCU_UART0_TX_3V3	MCU_UART0_TX_3V3	26
	MCU_UART0_RX_3V3	MCU_UART0_RX_3V3	26
	MCU_UART0_CTS_3V3	MCU_UART0_CTS_3V3	26
	MCU_UART0_RTS_3V3	MCU_UART0_RTS_3V3	26

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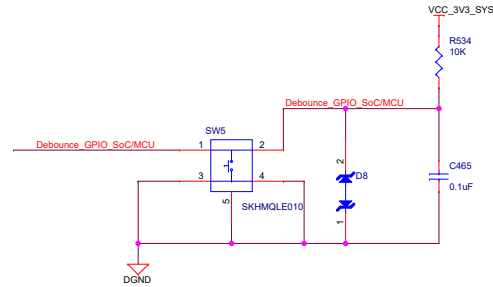
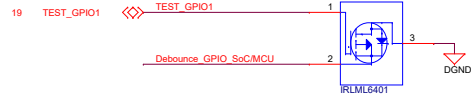
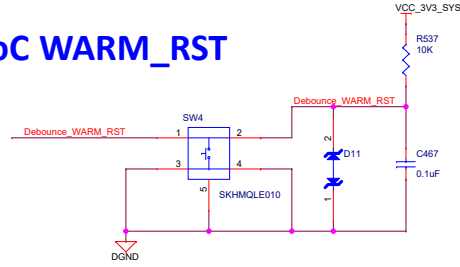
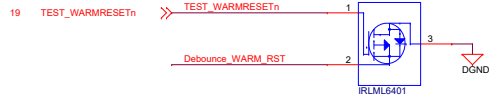


Title	MCU GENERAL & SAFETY CONNECTOR		
Size			
C	Variant Name = PROC101C(002) TMD5243GPEVM	Rev	
Date:	Monday, August 22, 2022	Sheet	34 of 40

SoC POR_RST

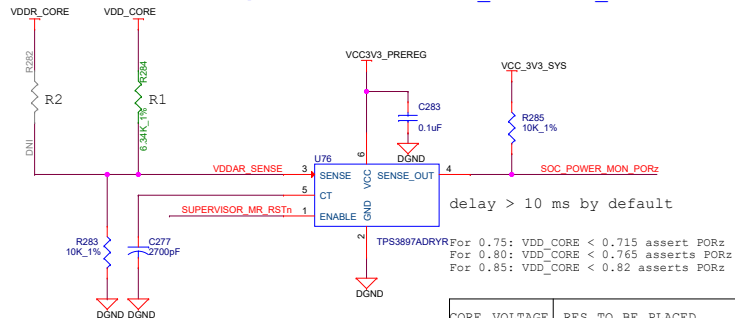


SoC WARM_RST



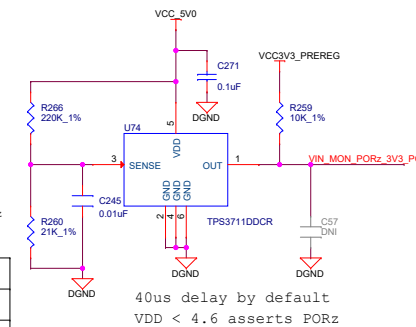
VOLTAGE SUPERVISOR

Core Voltage Monitor (VDDAR_CORE/VDD_CORE)

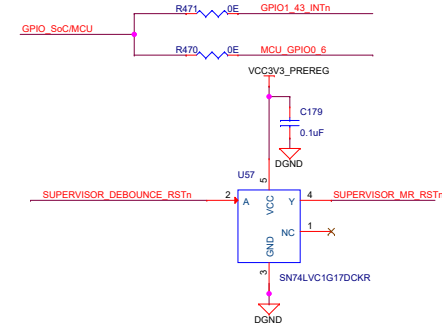
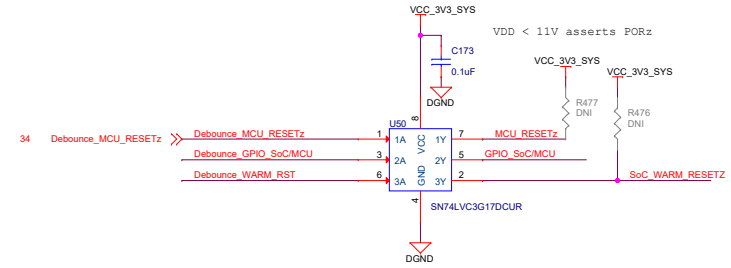


CORE VOLTAGE	RES TO BE PLACED
0.75V	R1 = 4.3K
0.80V	R2 = 5.23K
0.85V	R2 = 6.34K

5V OUTPUT MONITOR (VCC_5V0)

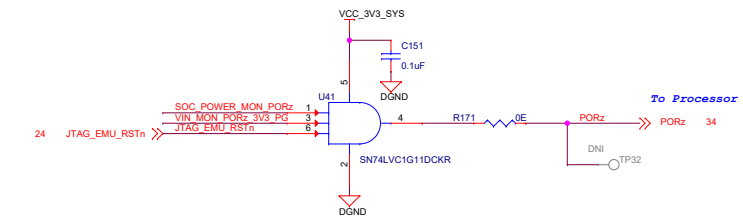


DEBOUNCE CIRCUIT



Off Page Connections

To Processor	VIN_MON_PORz_3V3_PG	VIN_MON_PORz_3V3_PG	37,39
	SoC_WARM_RESETz	SoC_WARM_RESETz	34
	GPI01_43_INTn	GPI01_43_INTn	29
	MCU_RESETz	MCU_RESETz	27,34
	MCU_GPI00_6	MCU_GPI00_6	34



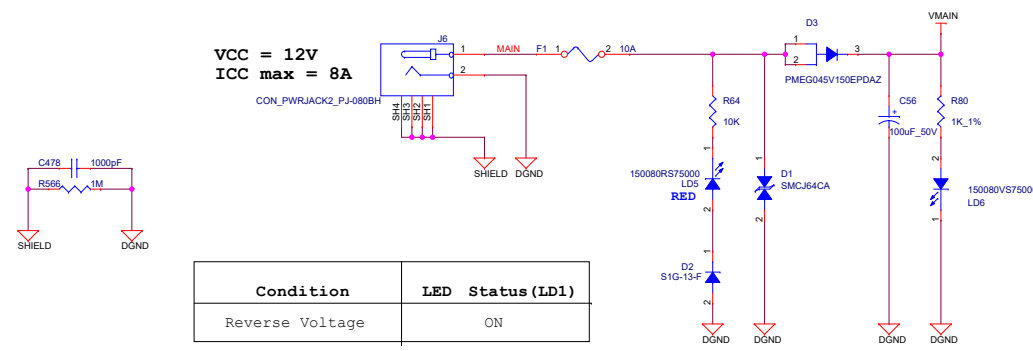
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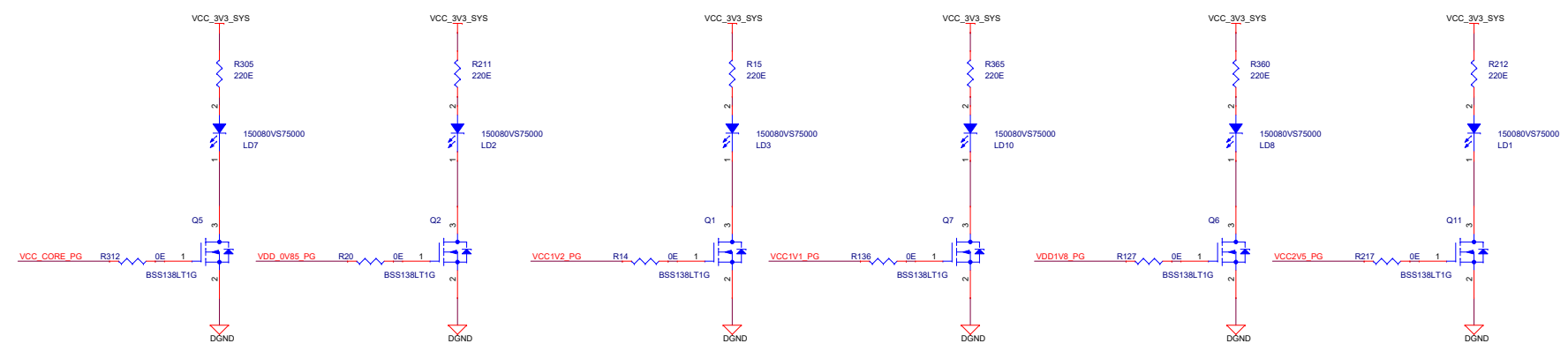
Title DEBOUNCE CIRCUIT & VOLTAGE SUPERVISOR

Size	Variant Name = PROC101C(002) TMD5243GPEVM	Rev
C		E2
Date:	Monday, August 22, 2022	Sheet 35 of 40

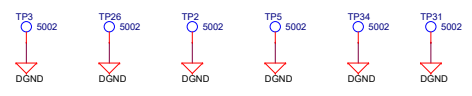
MAIN INPUT 12V DC



POWER INDICATION LED'S



Ground test points



Off Page Connections

VCC_CORE_PG	VCC_CORE_PG	37,38
VDD_0V85_PG	VDD_0V85_PG	38
VCC1V2_PG	VCC1V2_PG	38
VCC1V1_PG	VCC1V1_PG	38
VDD1V8_PG	VDD1V8_PG	39
VDD1V8_PG	VDD1V8_PG	38
VCC2V5_PG	VCC2V5_PG	39

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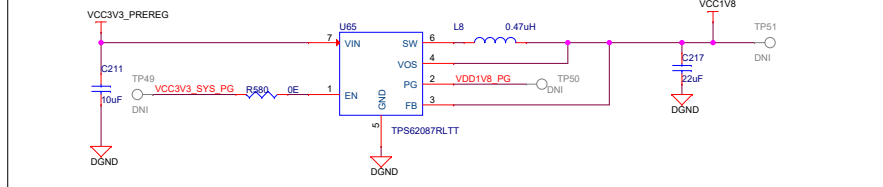


Title MAIN 12V POWERSUPPLY		
Size	Variant Name = PROC101C(002) TMD5243GPEVM	Rev E2
C		
Date: Monday, August 22, 2022	Sheet 36 of 40	

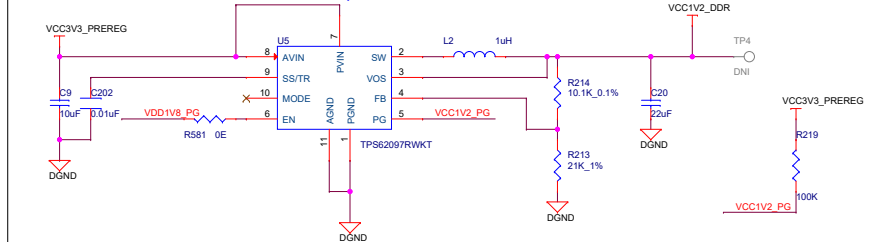
E

SoC POWER SUPPLY

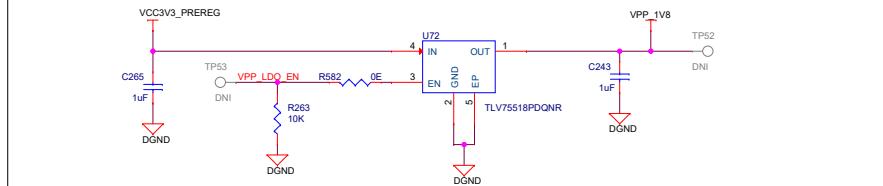
1.8V IO, 3.0AMPS SUPPLY



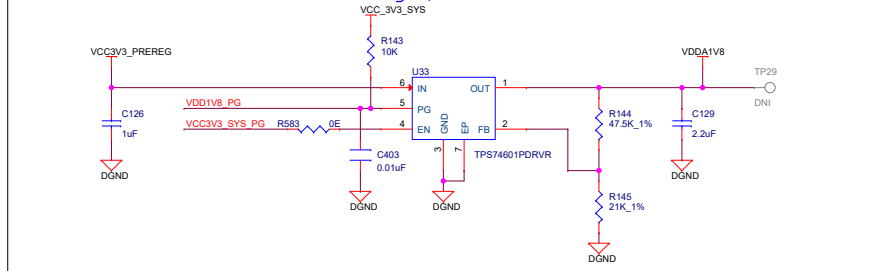
1.2V, 2.0AMPS SUPPLY



1.8V VPP, 0.15AMPS SUPPLY



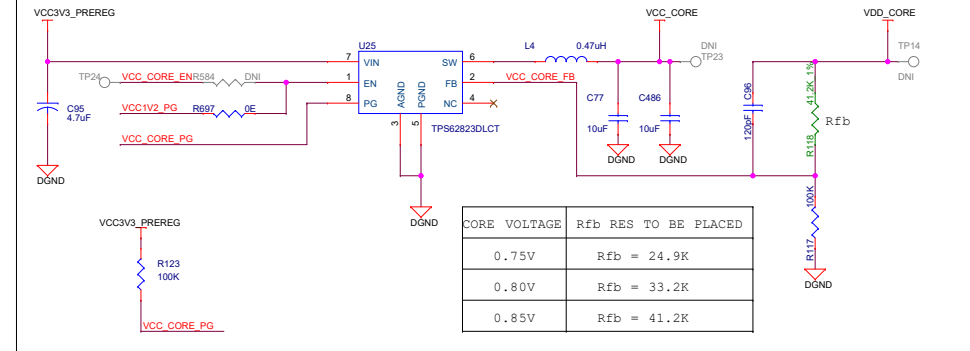
1.8V Analog , 1AMPS SUPPLY



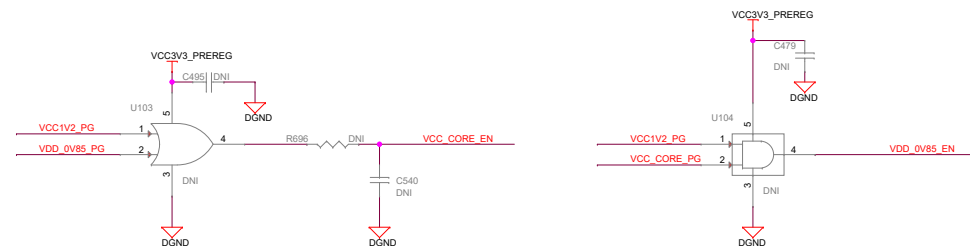
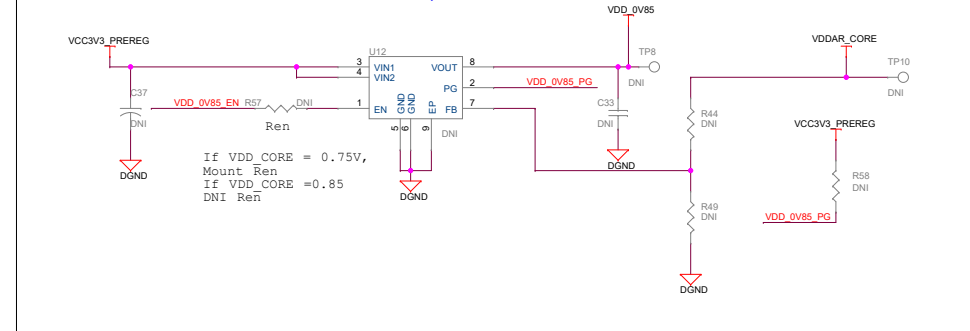
Off Page Connections

36.37	VCC_CORE_PG	VCC_CORE_PG
36	VDD_0V85_PG	VDD_0V85_PG
36	VCC1V2_PG	VCC1V2_PG
36	VDD1V8_PG	VDD1V8_PG
33	VPP_LDO_EN	VPP_LDO_EN
35,37,39	VIN_MON_PORz_3V3_PG	VIN_MON_PORz_3V3_PG
37,39	VCC3V3_SYS_PG	VCC3V3_SYS_PG

0.75 / 0.8 / 0.85V, 3.0AMPS SUPPLY



0.85 V, 1.5AMPS SUPPLY



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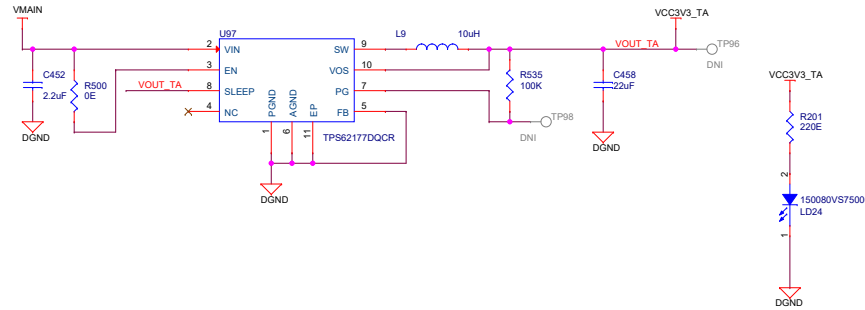


Title SoC POWER SUPPLY

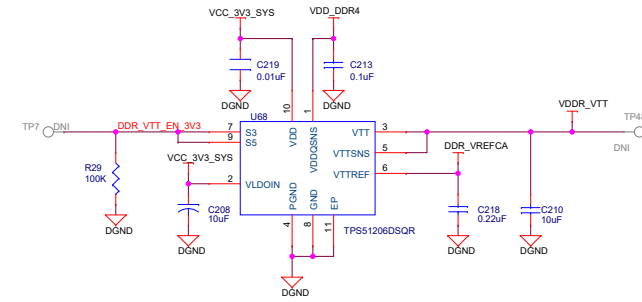
Size	Variant Name = PROC101C(002) TMD5243GPEVM	Rev
C		E2
Date:	Monday, August 22, 2022	Sheet 38 of 40

PERIPHERAL POWER SUPPLY

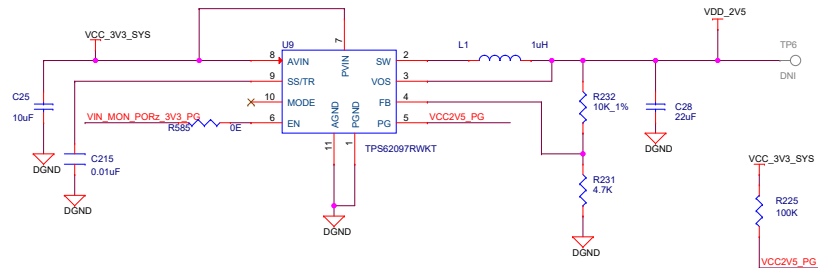
TEST AUTOMATION BOARD POWER



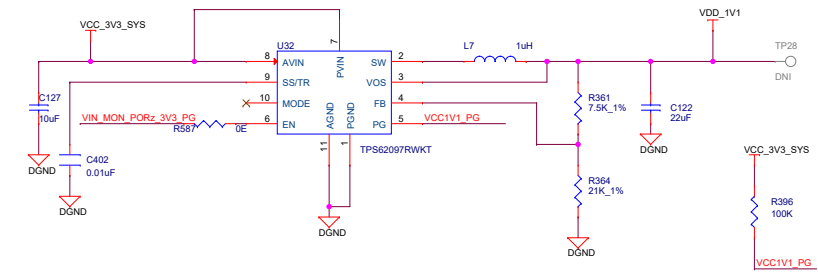
VTT SUPPLY FOR DDR4



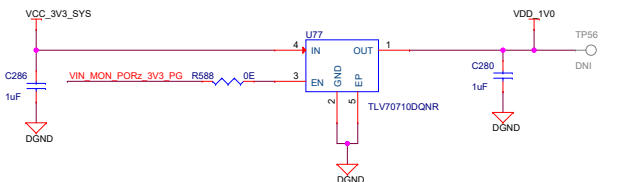
2.5V, 2.0AMPS SUPPLY



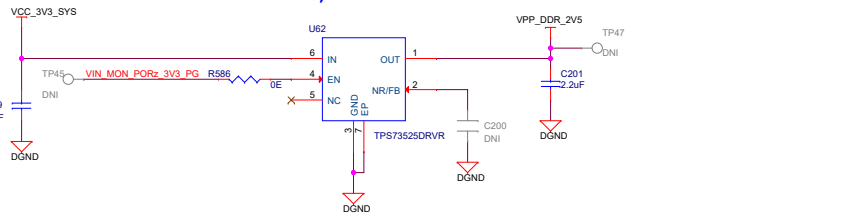
1.1V ETHERNET PHY POWER SUPPLY



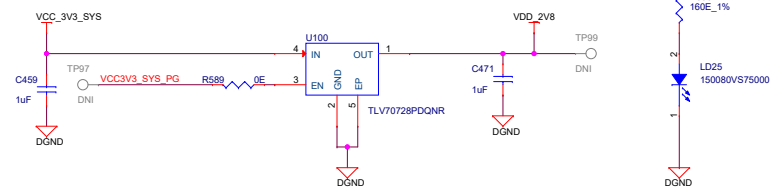
1.0V ETHERNET PHY POWER SUPPLY



2.5V, .5 AMPS SUPPLY



2.8V , 0.15AMPS SUPPLY



Off Page Connections

33	DDR_VTT_EN_3V3	DDR_VTT_EN_3V3
36	VCC2V5_PG	VCC2V5_PG
36	VCC1V1_PG	VCC1V1_PG
37,38	VCC3V3_SYS_PG	VCC3V3_SYS_PG
35,37	VIN_MON_PORz_3V3_PG	VIN_MON_PORz_3V3_PG

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Title PERIPHERAL POWER SUPPLY

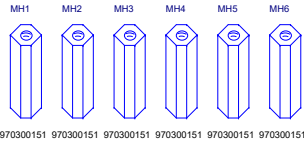
Size	Variant Name = PROC101C(002) TMD5243GPEVM	Rev
C		E2
Date:	Monday, August 22, 2022	Sheet 39 of 40

HARDWARE SCHEMATICS

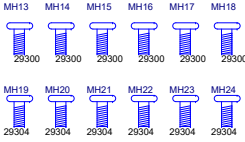
ASSEMBLY NOTES

- 1. All MSL components should be baked as per JEDEC standard.
- 2. PCB should be baked at 120 degree for 8 hours.
- 3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
- 4. These assemblies are ESD sensitive, ESD precautions shall be observed.
- 5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
- 6. Provide serial numbers to the assembled boards for identification.
- 7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

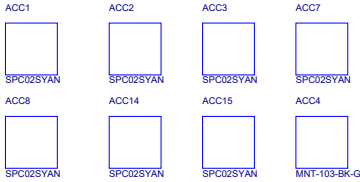
STANDOFFS



SCREWS



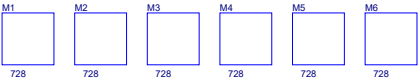
JUMPERS



WASHER'S



RUBBER FEET



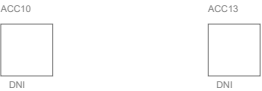
FIDUCIALS



TI EVM FLYERS



Socket & Processor as Accessories



BARE PCB



LABELS

Board Serial No.



Assembly Revision

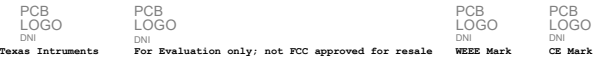


ORDERABLE PART NO



Orderable part number	
Variant	Label Text
001	TMDS64GPEVM
002	TMDS243GPEVM
003	TMDS64HSEVM
004	TMDS64EVM
005	TMDS243EVM

LOGOS



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Title HARDWARE SCHEMATICS

Size	Variant Name = PROC101C(002) TMDS243GPEVM	Rev
C		E2
Date:	Monday, August 22, 2022	Sheet 40 of 40